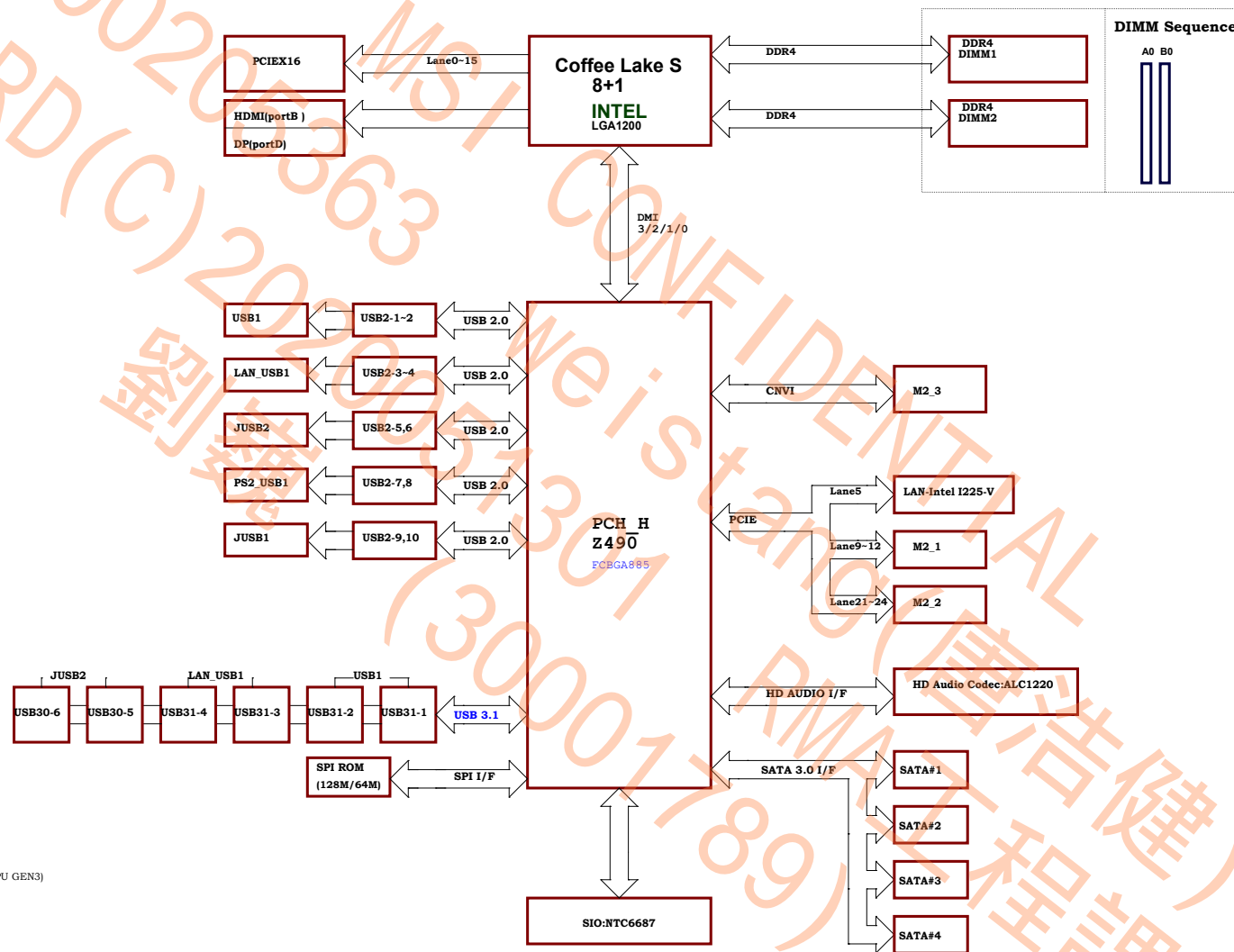


TITLE		Page	MS-7C77		ITX:170*170
Cover Sheet		1			Ver: 1.3
Block Diagram		2	CML Platform		
CPU-Memory, CPU-Control/MISC/CFG/Audio		3,4	CPU: Comet lake S		System Chipset: Z490 PCH_H
CPU-PEG/Display/RSVD		5	LGA1200		
CPU-Power,CPU-GND		6,7	CPU POWER PAK *8 Phase		
DDR4 DIMM1&DDR4 DIMM2 & DDR4 POWER		8,9,10,11	GT POWER PAK *1 Phase		
PCH-LPC/SPI/SMBUS/MISC		12	Onboard Chip: SIO:NTC6687		
PCH-Audio/Display/Clock		13	HD Audio Codec:ALC1220		
PCH-DMI/PCIE/USB/SATA		14	LAN-Intel I225-V		
PCH-GPIO/RSVD/CNVI		15	Flash ROM: SPI 128 MB X1		
PCH-Power/Gnd/Strip		16,17,18	Main Memory: DDR4 * 2 (Dual Channel)		
PCIE SLOT-CPU(X16)		19	ACPI:		Power:
SIO-NCT6687D		20,21	5VDAUL:uP7501		VCORE/GT/SA - ISL69269
SPI ROM BIOS/ FAN VBAT/CLR COMS		22,23,24,25	5VDIMM:uP7501		VCCIO -RT8125E
MCU JRAINBOW/DEBUG LED		26	3VSB:TPS566235		VCCST/VCCSTG-MP2333
AUDIO - ALC1220P		27,28	3VDSW:GS7133		VCCPLL/VCCPLL_OC-GS7133
TR DP / PD		29,30,31,32	SIO_3VA:GS7116		DDR - RT8231
LAN - INTEL I255V		33			PCH(1.05V) - RT8125E
Rear LAN USB3.1&USB2.0		34			1P8_VSB - GS7133
Rear-USB31 TYPEA+TYPE C/Front USB 3.2/2.0		35,36	Expansion Slots:		
Front USB31 TYPE C / USB POWER		37,38	PCI Express (X16) Slot * 1		
M2 Connector/SATA/CNVI		39,40,41,42			
HDMI Connector/DP		43,44			
ACPI CONTROLLER		45			
PWR-ISL69269/CORE-PH1-8/GT PH1/SA PH1		46,47,48			
PWR-VCCIO-RT8125E/PWR-VCCST/PLL		49,50			
DDR-RT8231/VPP25-MP2333		51,52			
PCH RT8125E/1P8_VSB/PWR-VRM/PCH Sequence		53,54			
OV-NCT3933/ATX F_Panel		55,56			

MS-7C77 Block Diagram



Slot Sequence:
PCIe X16 (By CPU GEN3)



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MS-7C77

Size	Document Description
Custom	03 CPU-Memory

Rev	1.3
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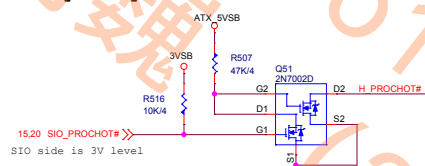


OR:1
0.1uF:1
1uF:0
4.7uF:0
10uF:0
22uF:0

CFG Strap

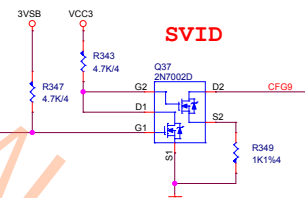
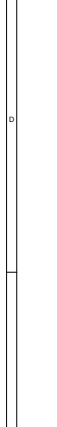
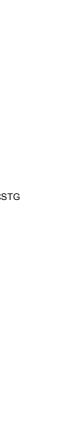
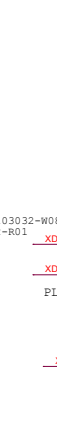
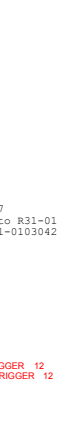
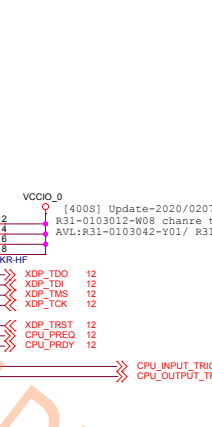
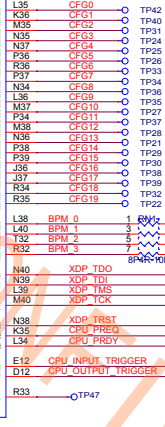
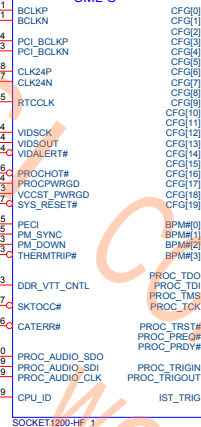
CFG Table		
HIGH	LOW	Intel
0 (Default)Normal Operation	stall	PCU PLL lock
1	REVERSE	REV0
2	REVERSE	PCU LANE REVERSAL
3	REVERSE	REV0
4	ENABLE	REV0
5	ENABLE	PCU_CFGSEL[0]
6	ENABLE	PCU_CFGSEL[1]
7	ENABLE	PCU_CFGSEL[2]
8	ENABLE	PCU_CFGSEL[3]
9	ENABLE	PCU_CFGSEL[4]
10	PRESENT	NO PRESENT
11	PRESENT	NO PRESENT
12	PRESENT	NO PRESENT
13	PRESENT	NO PRESENT
14	PRESENT	NO PRESENT
15	PRESENT	NO PRESENT
16	PRESENT	NO PRESENT
17	PRESENT	NO PRESENT
18	PRESENT	NO PRESENT
19	PRESENT	NO PRESENT

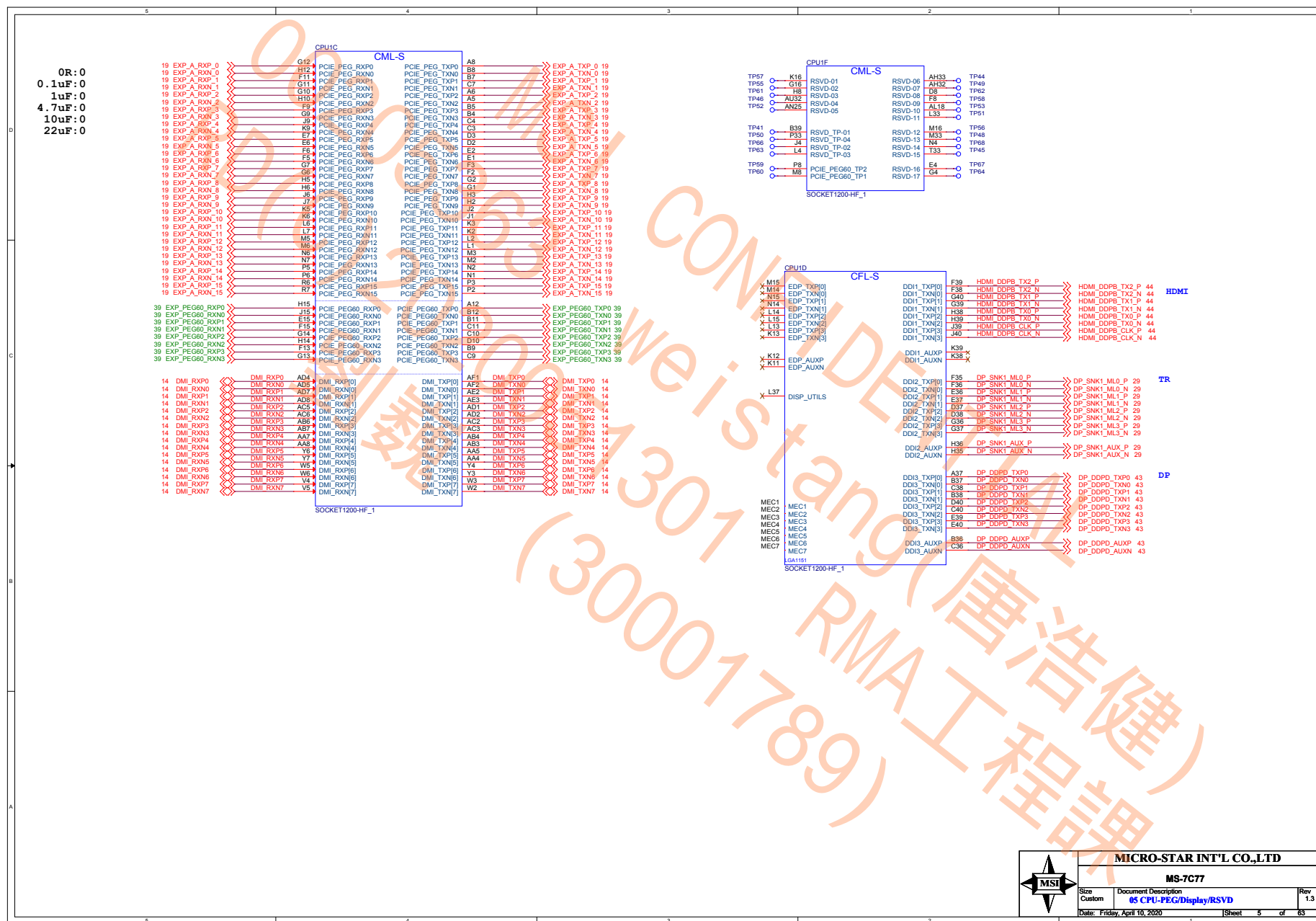
Temperature protection MP BOM remove



15.20 SIO_PROCHOT#
SIO side is 3V level

CML-S





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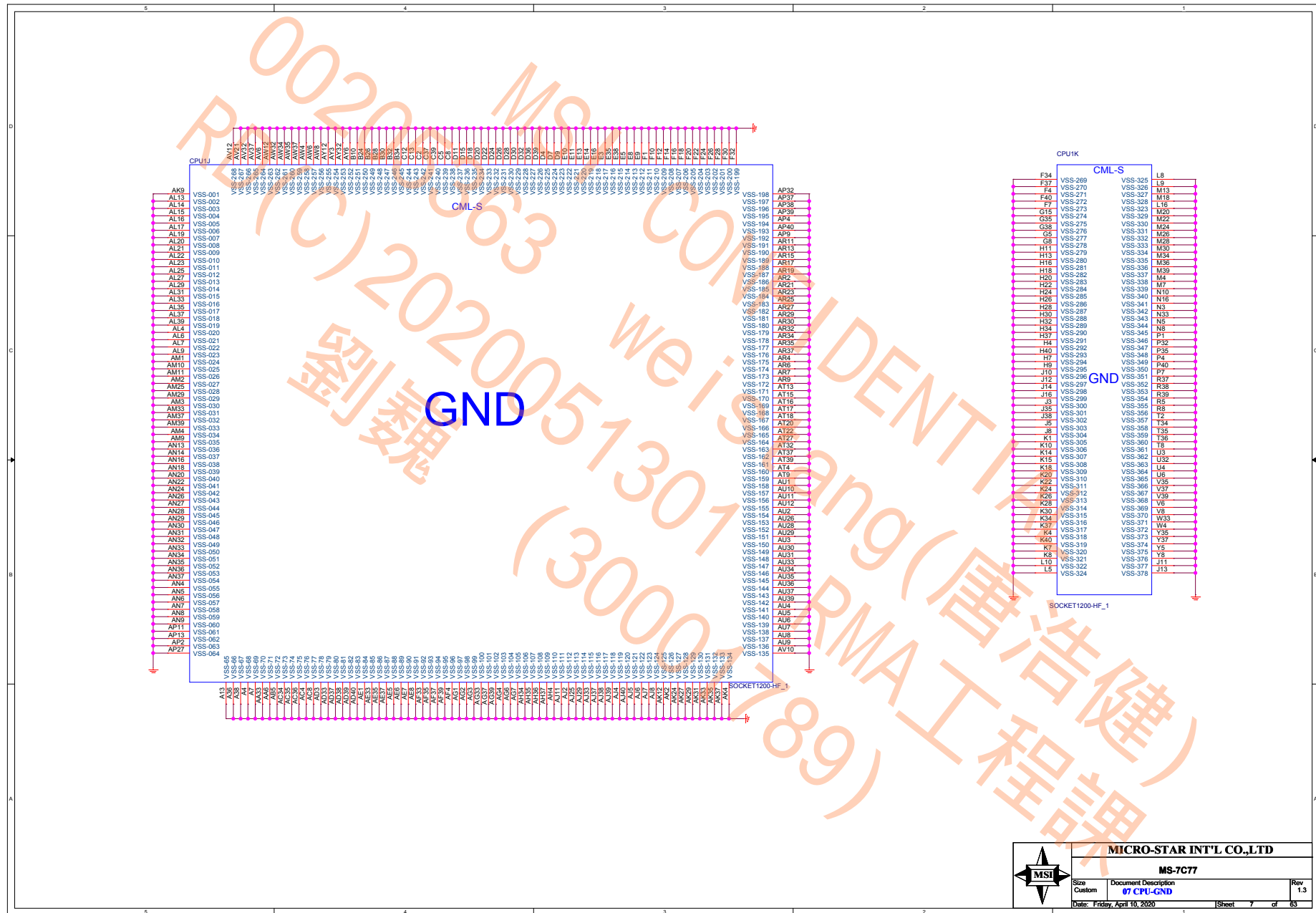
MS-7C77

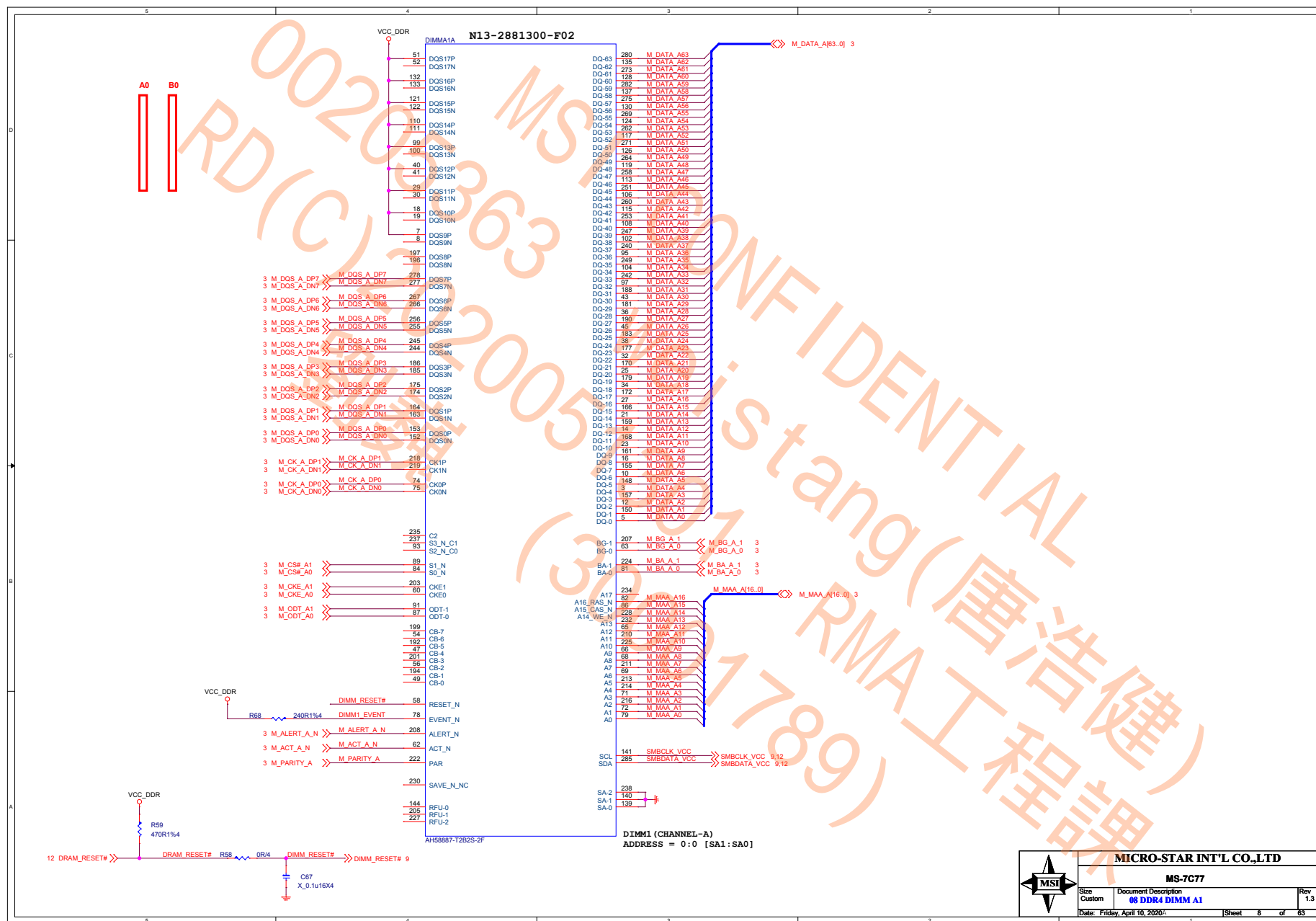
Size Custom	Document Description 05 CPU-PEG/Display/RSVD
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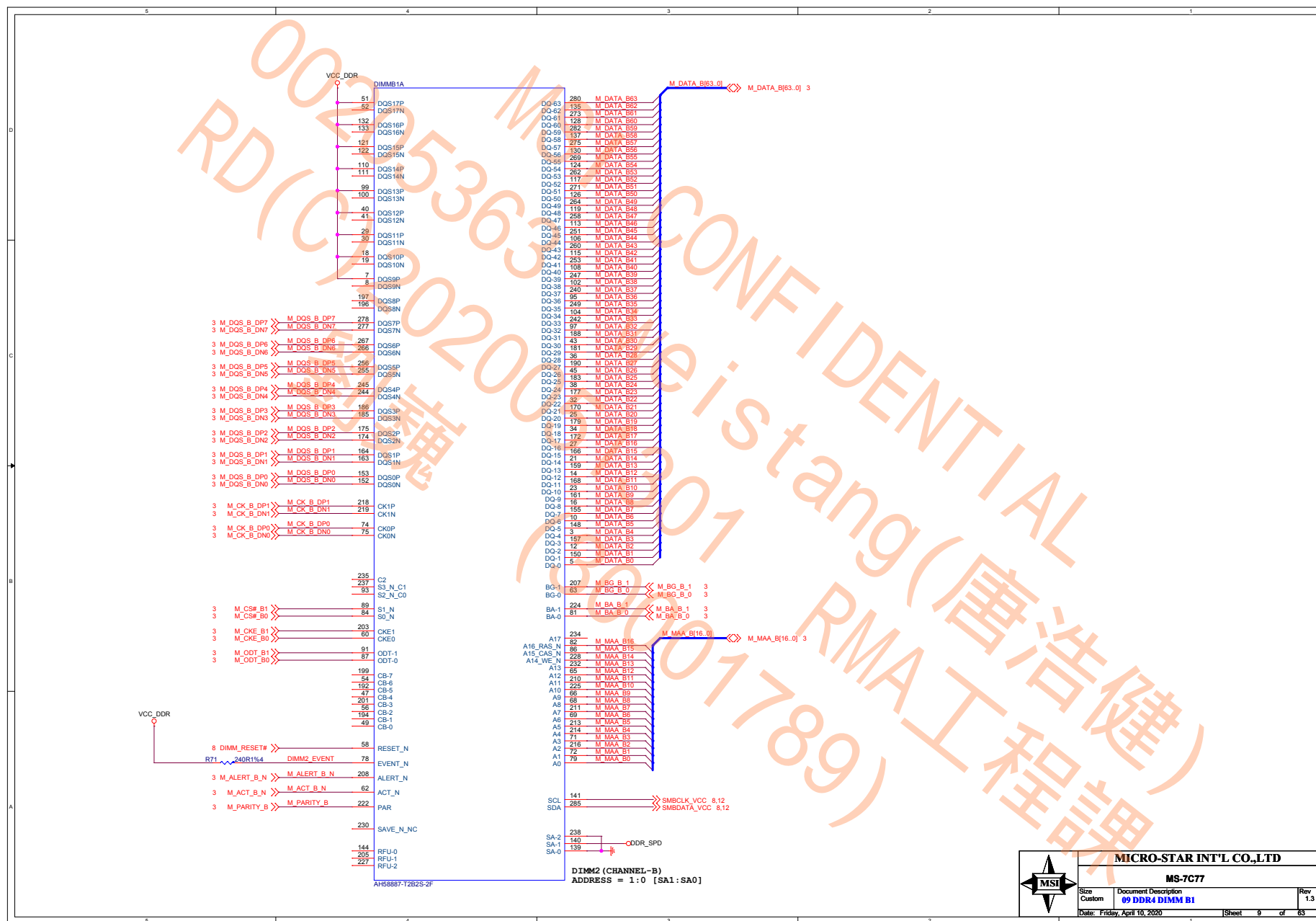
Rev	1.3
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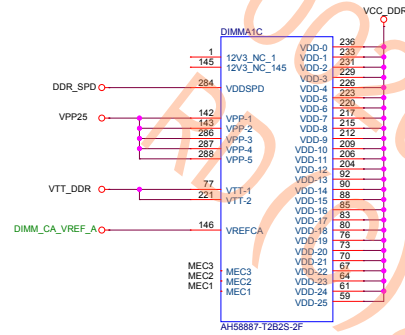
Date: Friday, April 10, 2020





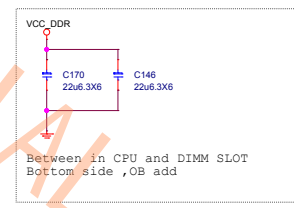
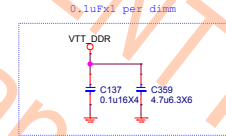
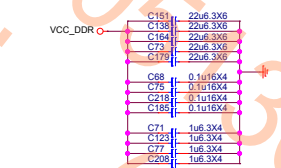
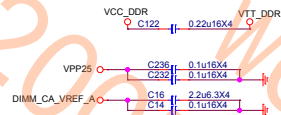
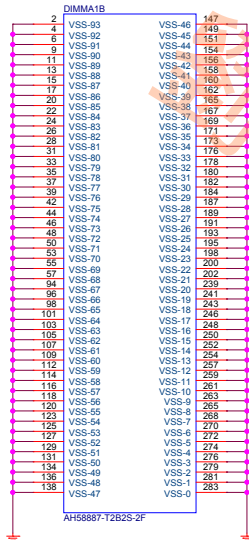
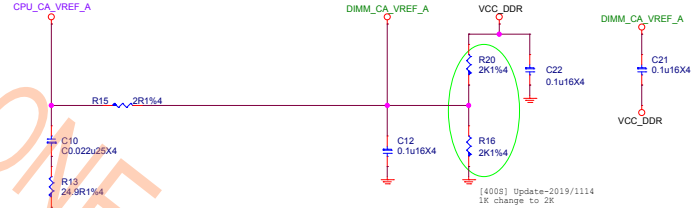
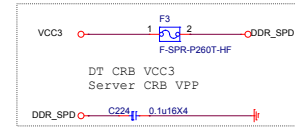


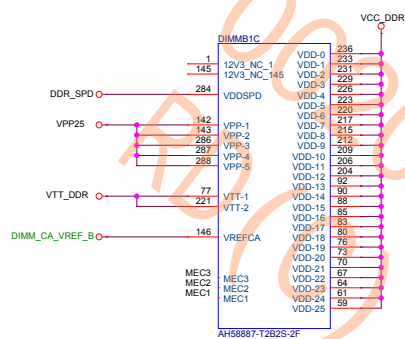




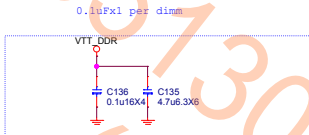
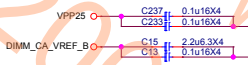
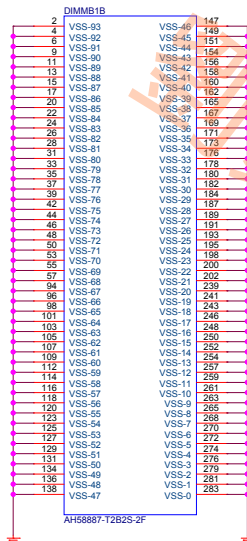
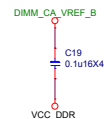
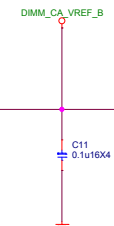
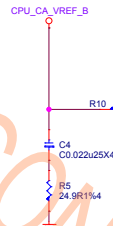
0R:0
0.1uF:12
1uF:4
4.7uF:1
10uF:0
22uF:7

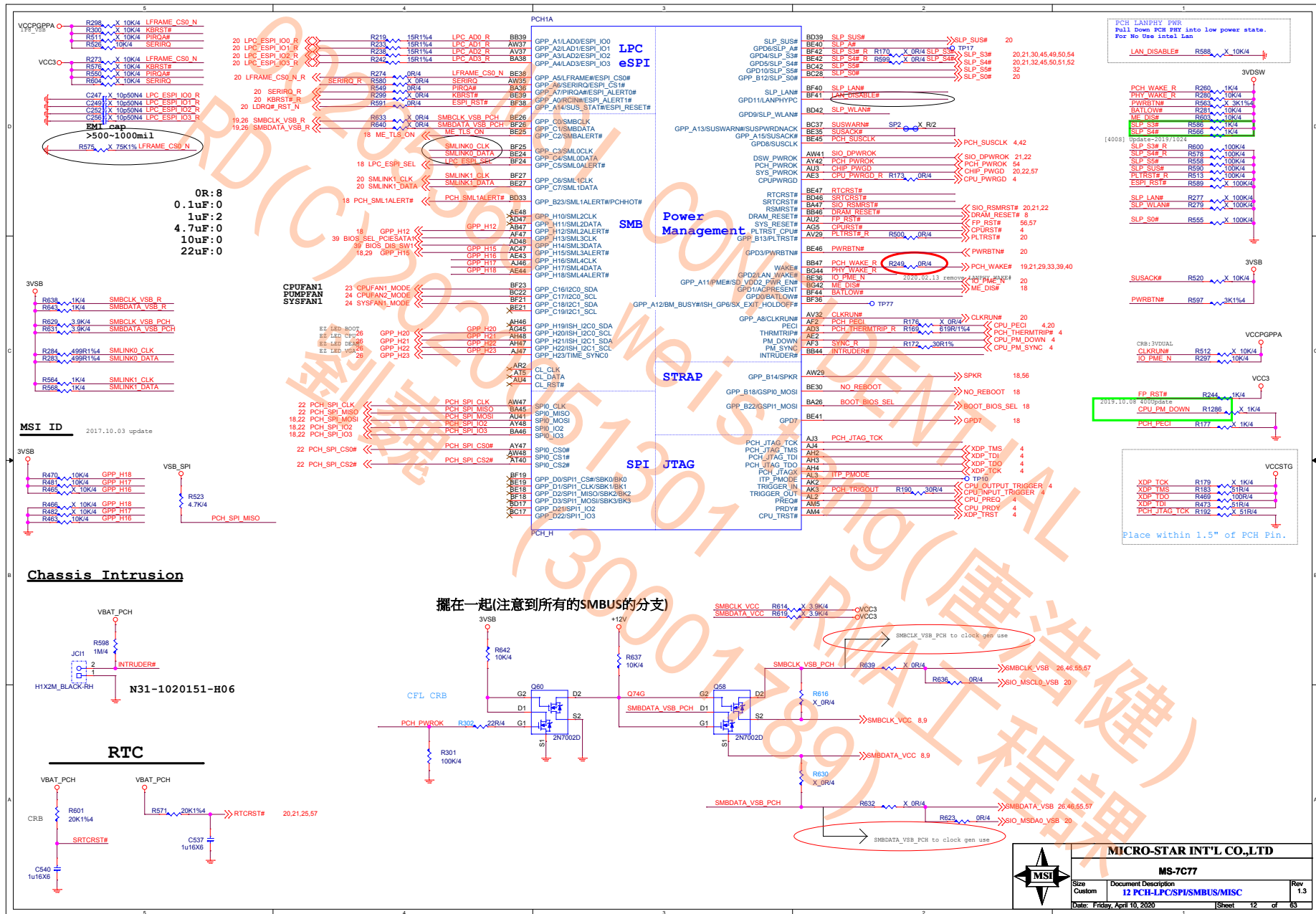
DIMM SLOT PN BY SPEC

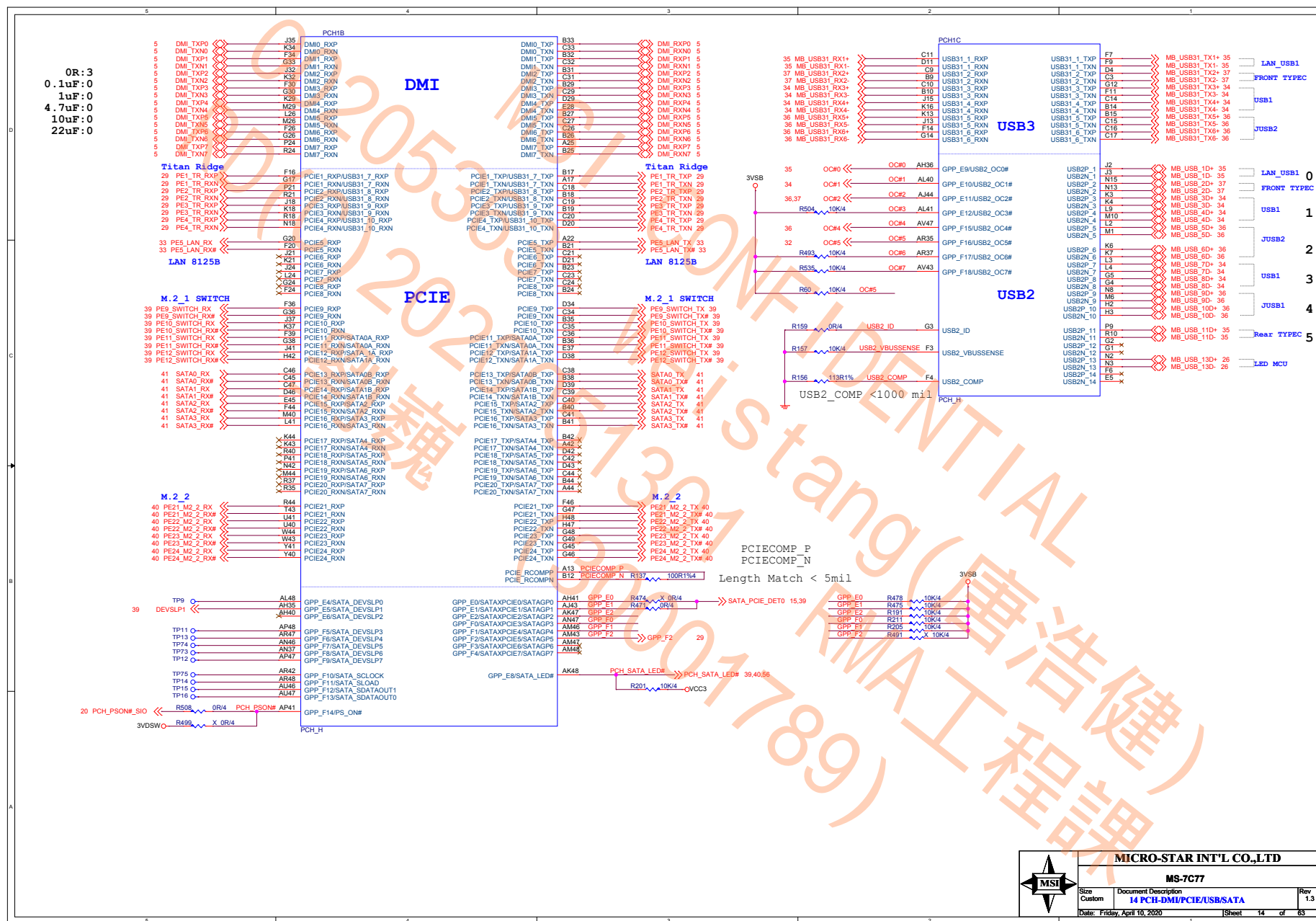


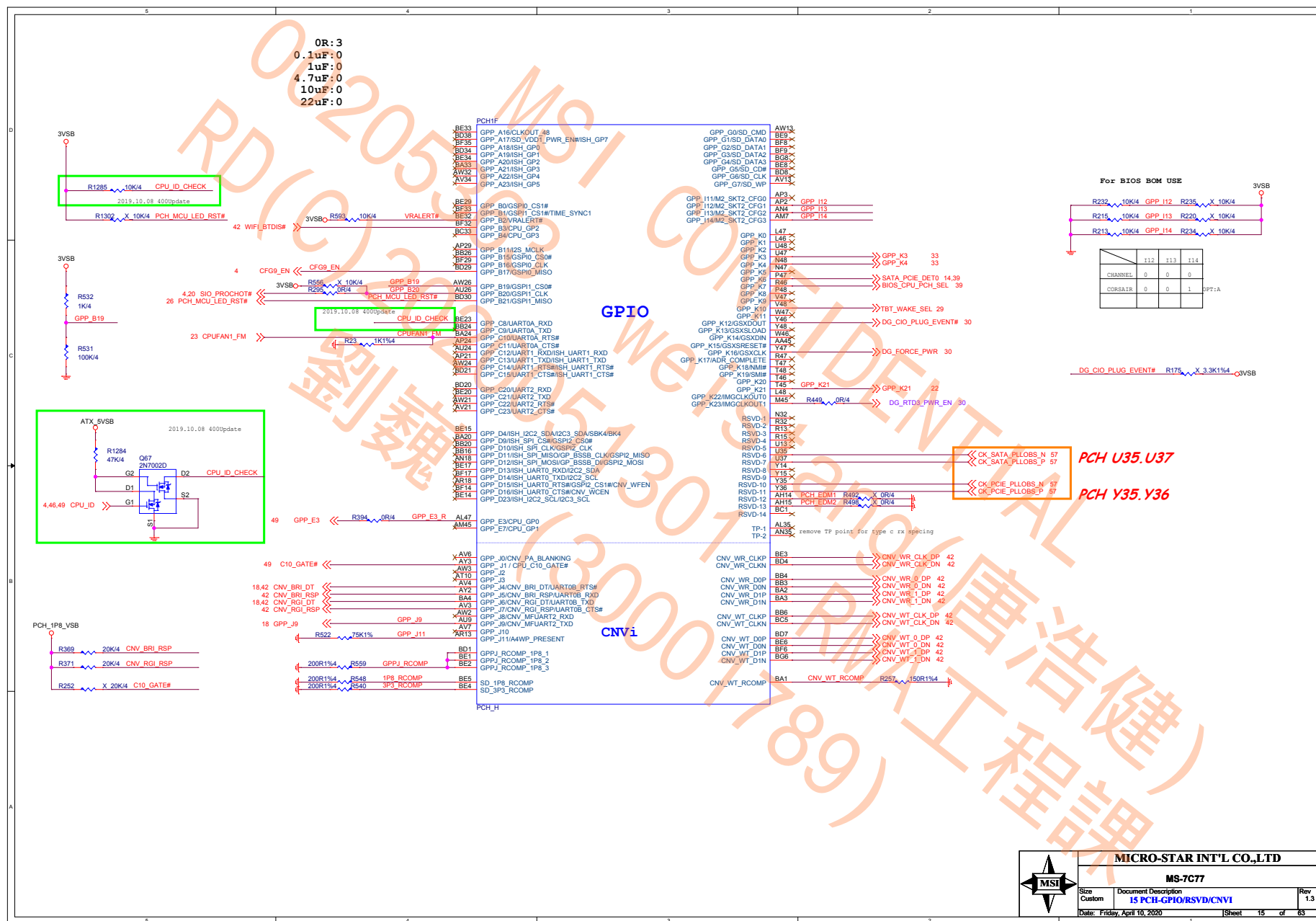


OR:0
0.1uF:11
1uF:4
4.7uF:1
10uF:0
22uF:5



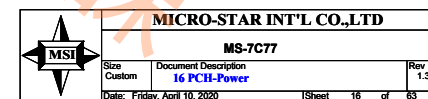






```
Base 7.169A
Base other 1.089A
DMI Gen3 0.5A
PCIE Gen3 1.602A
USB3.1 Gen1 1.062A
SATA3.0 0.668A
```

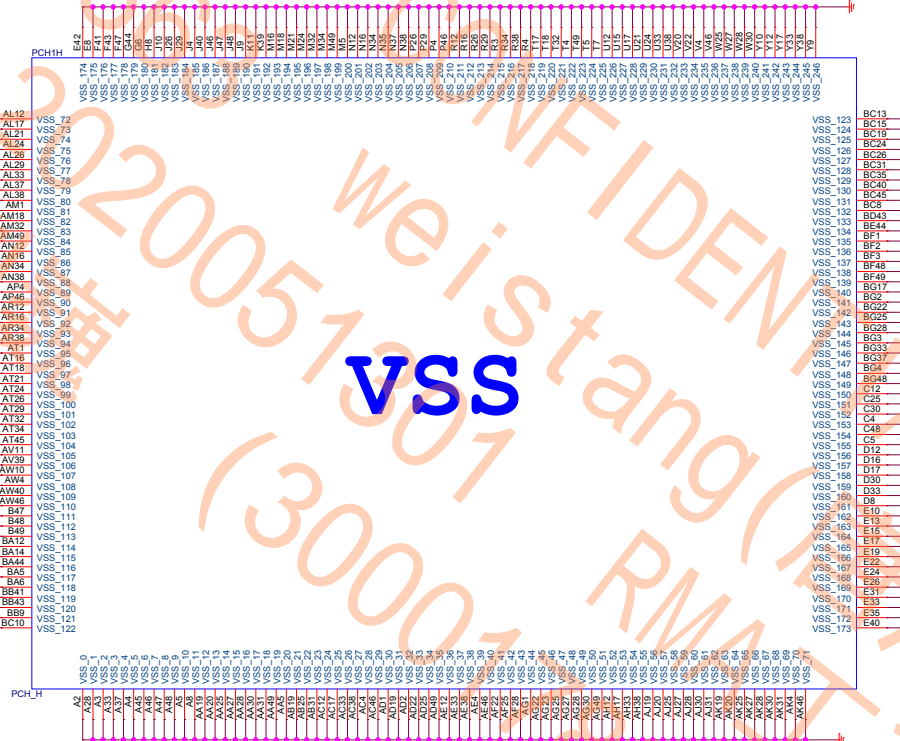
0R: 5
0.1uF: 18
1uF: 17
4.7uF: 0
10uF: 2
22uF: 6



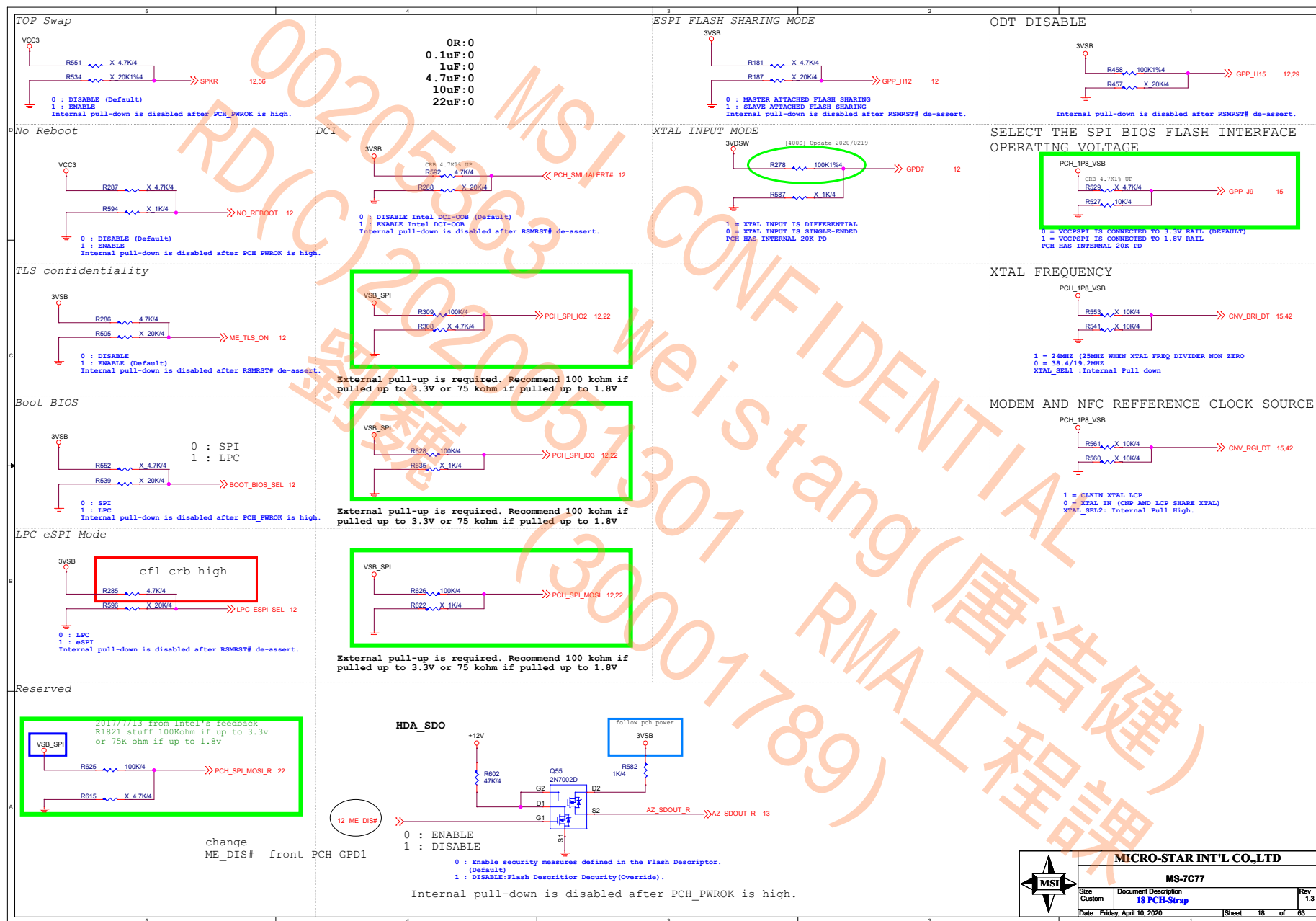
002051301 RD(C) MS I 20051301 we istang (30004 RM (30004) 002051301 RD(C) MS I 20051301 we istang (30004) 002051301 RD(C) MS I 20051301 we istang (30004)

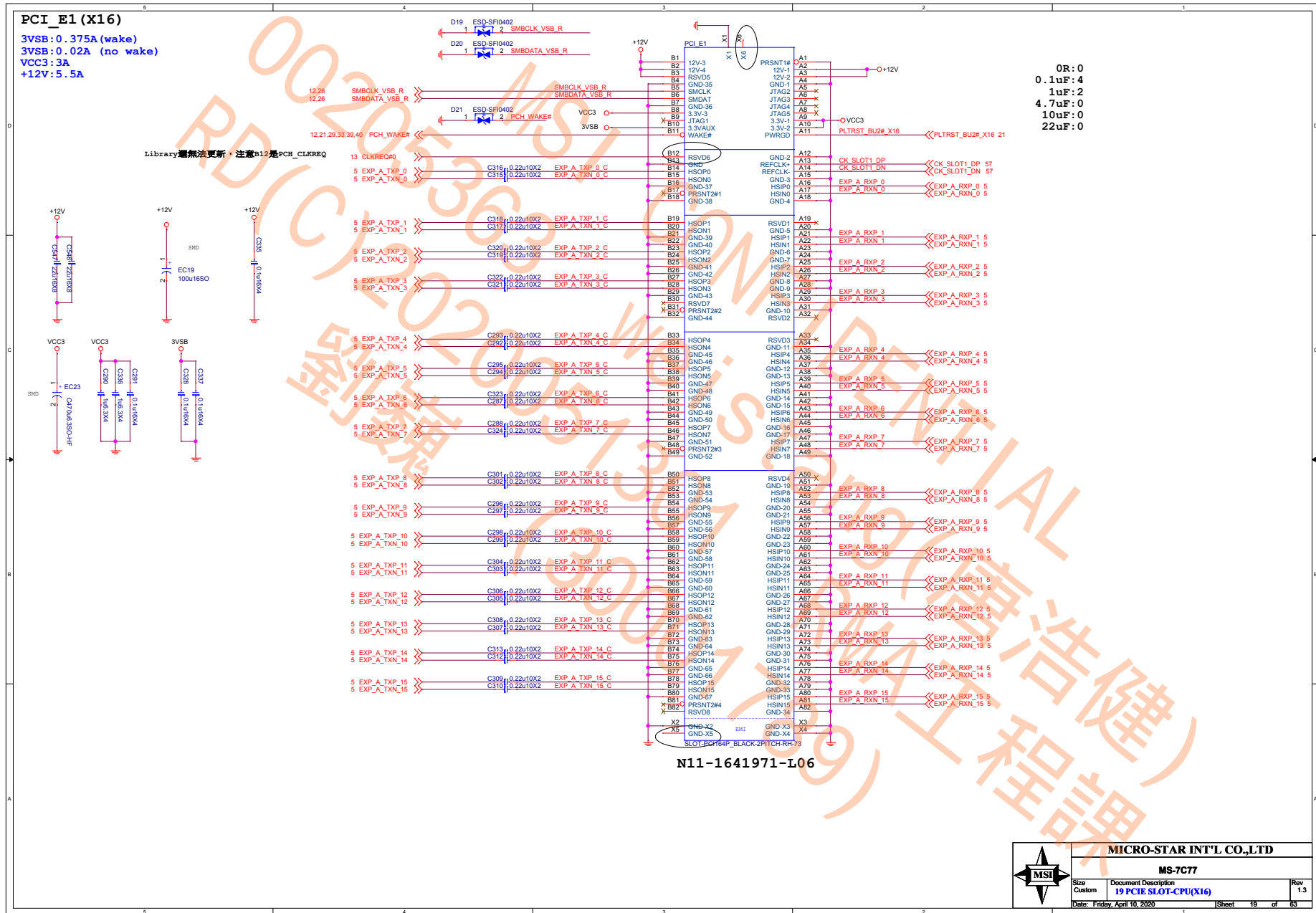


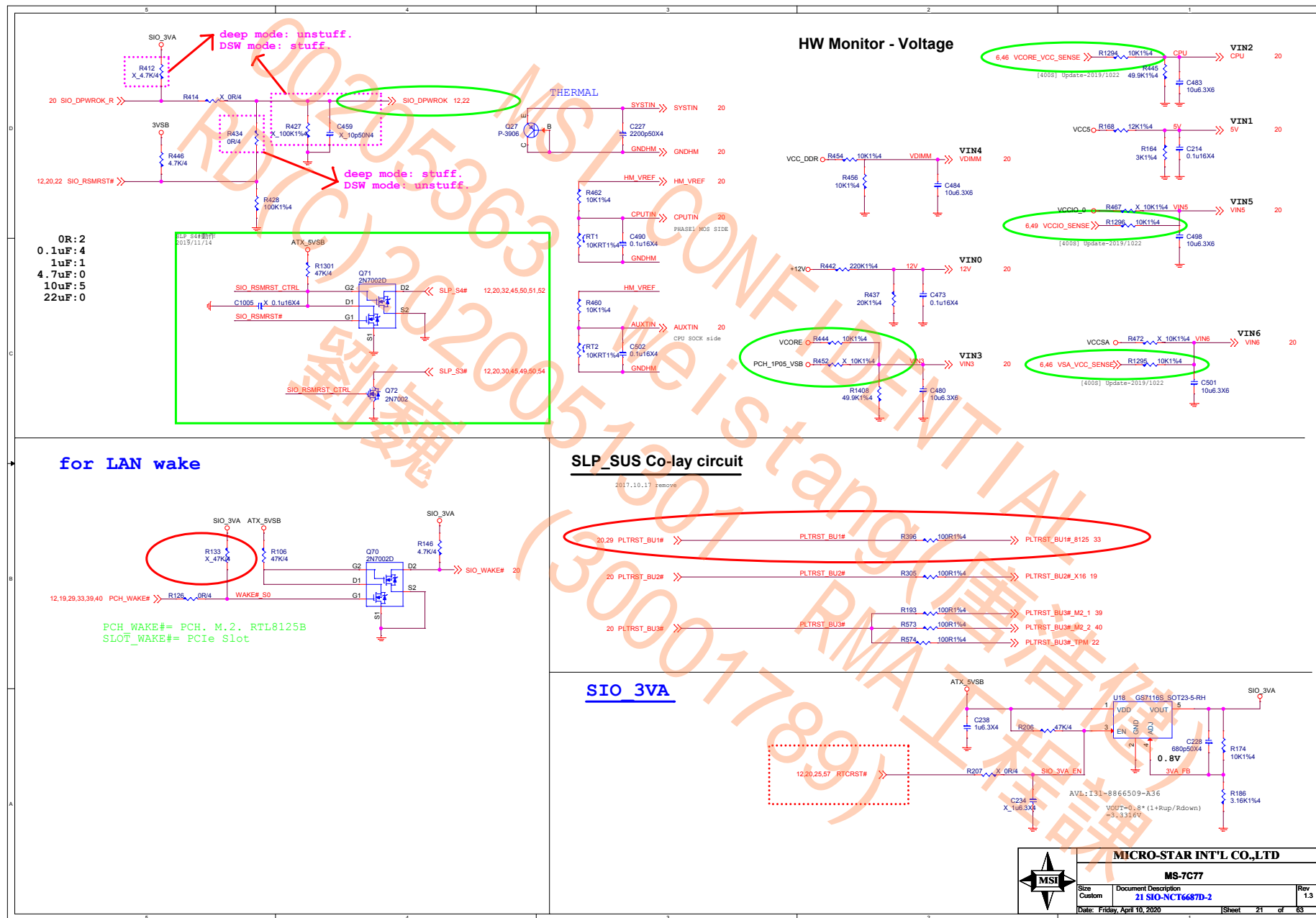
VSS



MICRO-STAR INT'L CO.,LTD		
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Timing diagram for SPI SW_SEL signal. The diagram shows the relationship between ATX_5VSB, CHIP_PWGD, SIO_DPWRCK, VSB_ENABLE#, and SIO_RSMRST# signals and the SPI_SW_SEL signal. SPI_SW_SEL is a square wave that transitions from high to low at approximately 12.20 ns, coinciding with the falling edge of SIO_RSMRST#. The signal remains low until approximately 20.45 ns, then transitions back to high. The diagram includes labels for R313 (10K/4) and R318 (100R1%4) resistors.

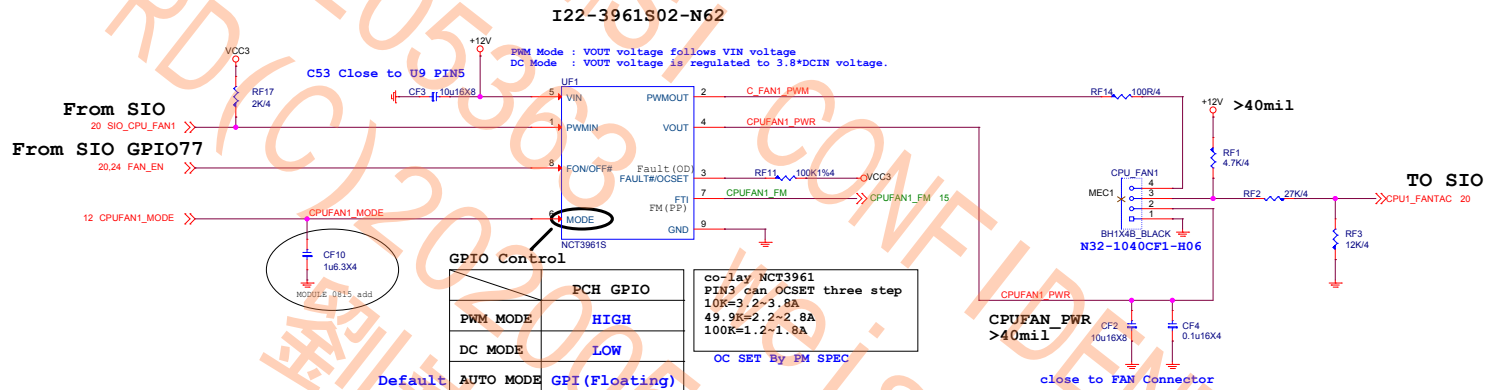


TYPE N : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

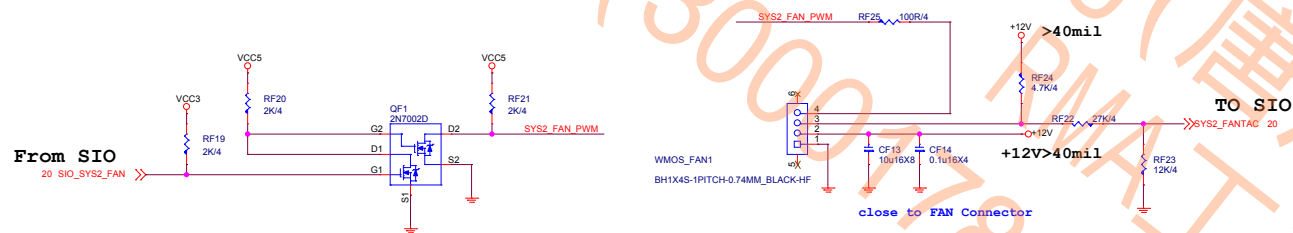
2.FM:BIOS can read FAN PWM/DC MODE

0R:0
0.1uF:2
1uF:1
4.7uF:0
10uF:3
22uF:0



2019/11/11 add real IO fan

TYPE O : 4 PIN FAN ONLY PWM MODE



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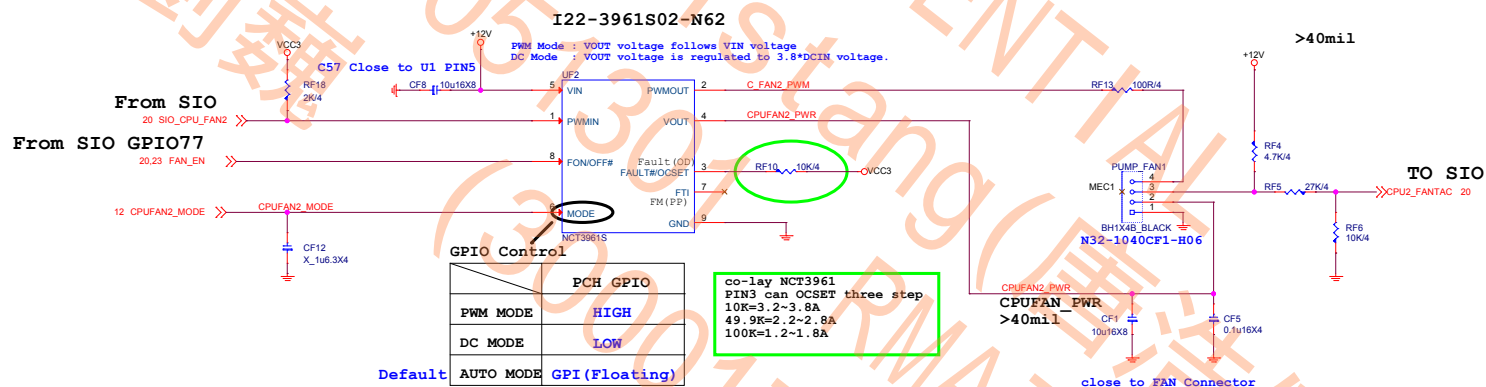
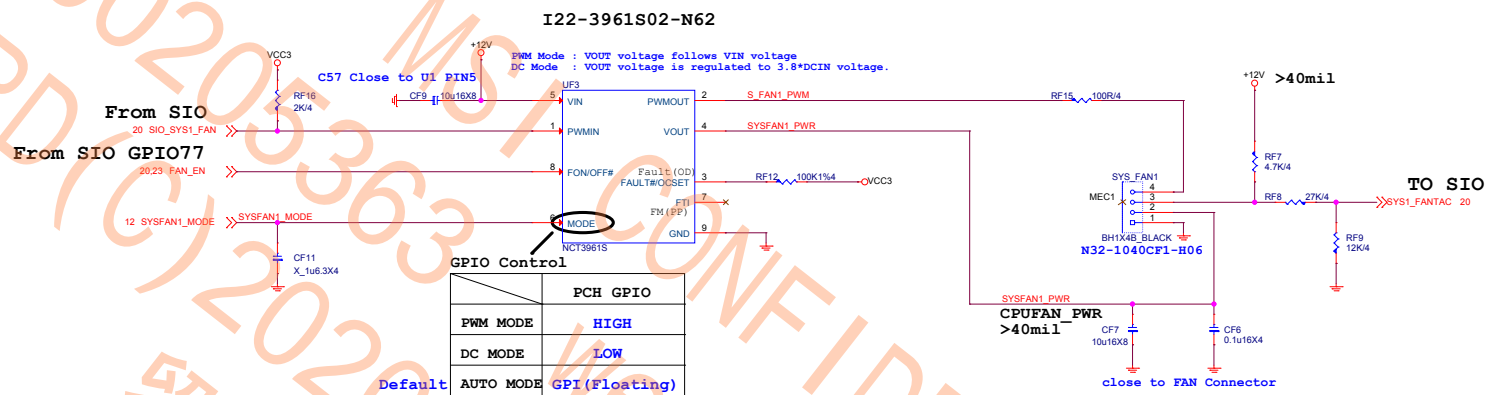
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Size Custom Document Description 23 FAN CPUFAN1 N Rev 1.3
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TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can switch PWM/DC MODE

0R:2
0.1uF:2
1uF:0
4.7uF:0
10uF:4
22uF:0



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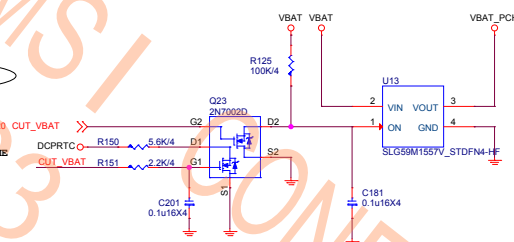
Size Custom Document Description 24 FAN PUMP/SYS M

Date: Friday, April 10, 2020 Sheet 24 of 63

Rev 1.3

[illegible]

VBAT VBAT_PCH



Close to PCB

S-BAT54C_SOT23

BAT1_1

BAT1_2

BAT1_3

BAT_3V

3VDSW

SIO_3VA

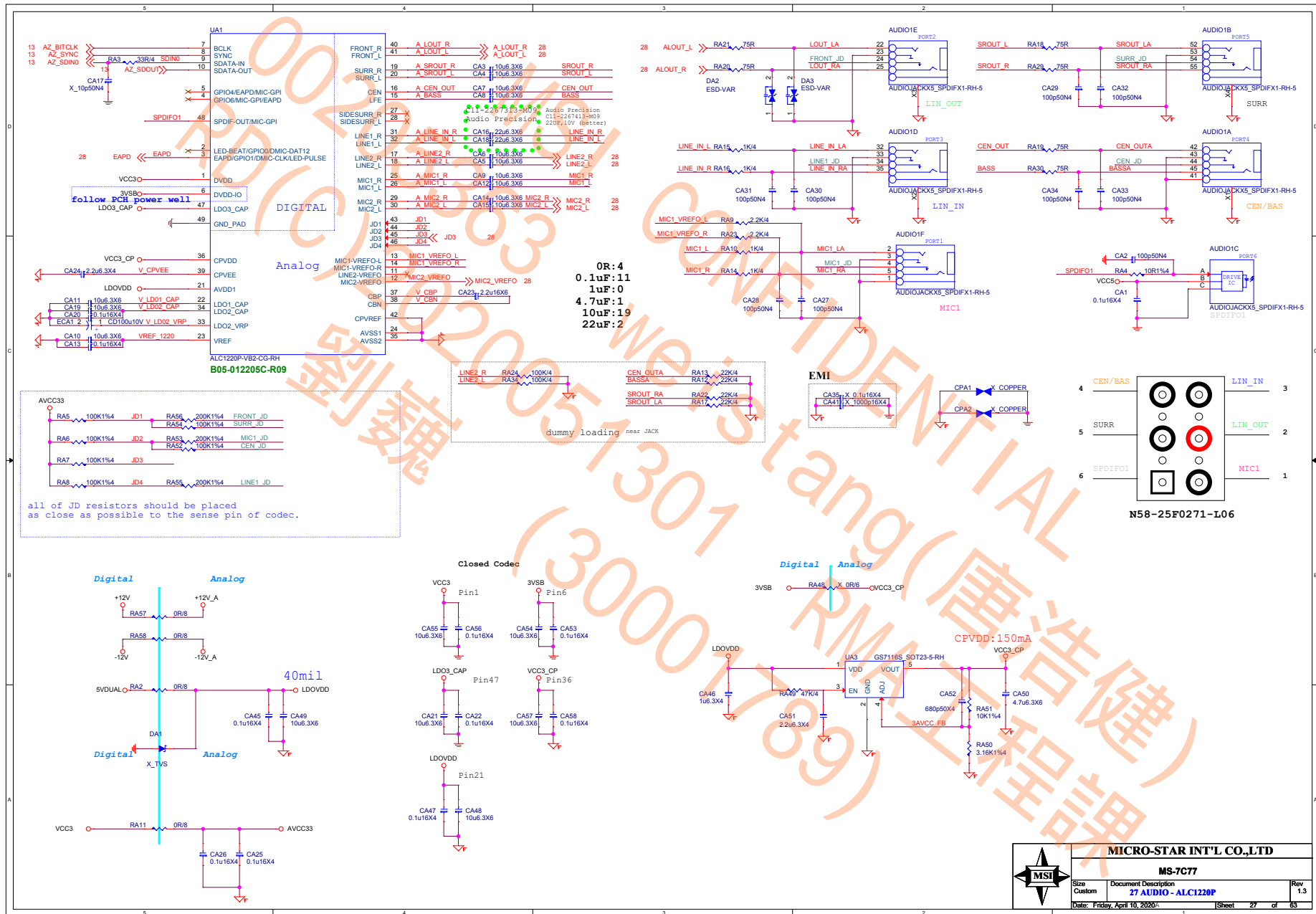
VBAT

R107 1K1%4

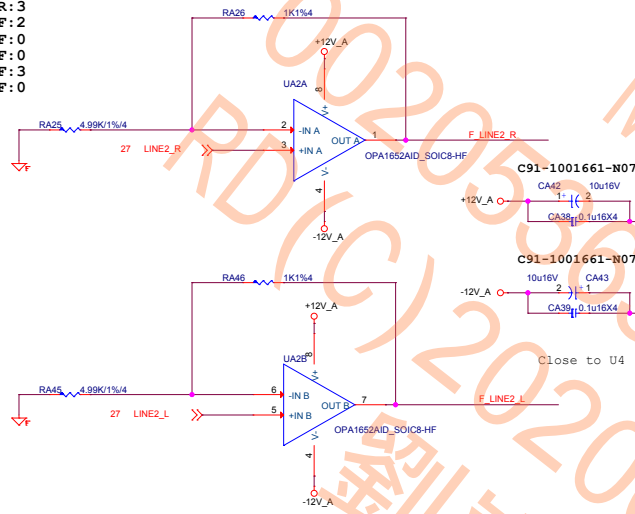
R129 0R/4

C183 0.1u16X4

C177 1u6.3X4



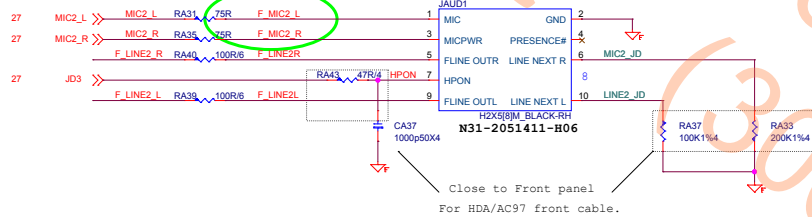
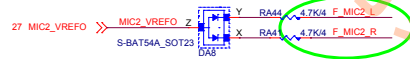
0R:3
0.1uF:2
1uF:0
4.7uF:0
10uF:3
22uF:0



C91-1001661-N07

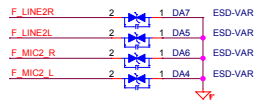
C91-1001661-N07

Close to U4

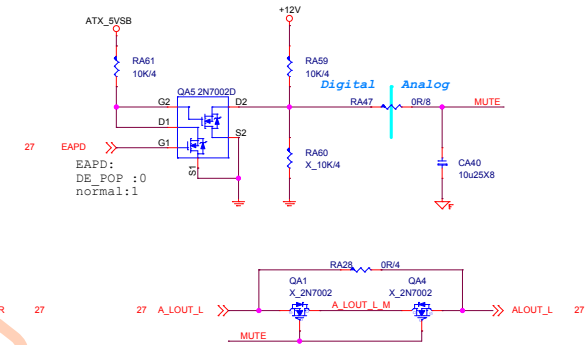


Close to Front panel
For HDA/AC97 front cable.

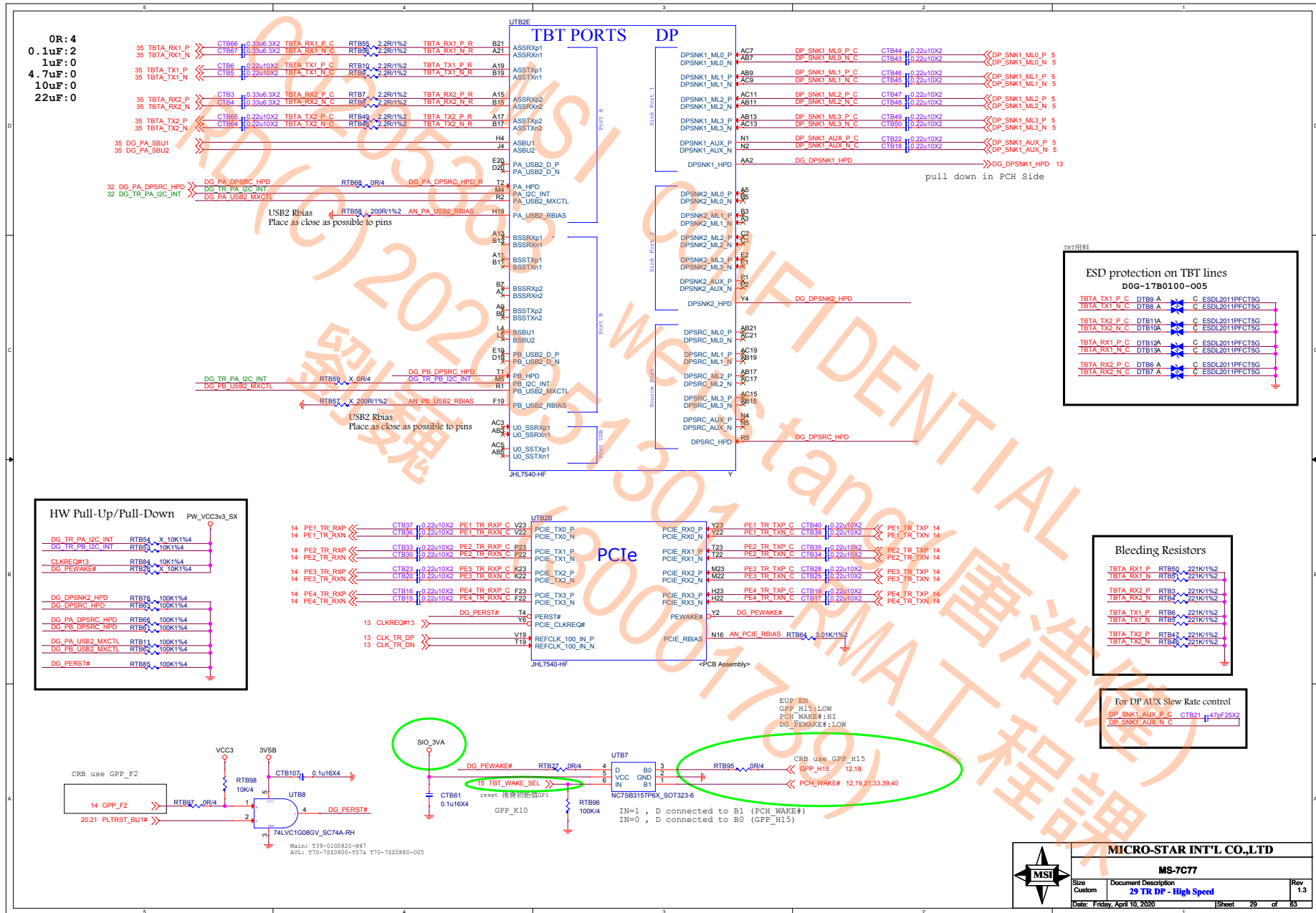
Close to Jack
ESD protect



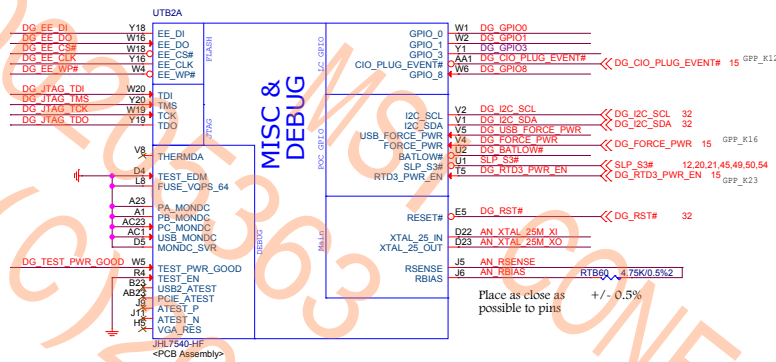
De-POP circuit



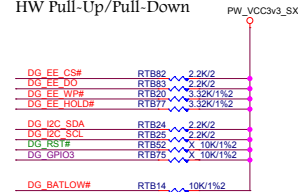
MICRO-STAR INT'L CO.,LTD			
MS-7C77			
Size	Document Description	Rev	
Custom	28 AUDIO - depop circuit	1.3	
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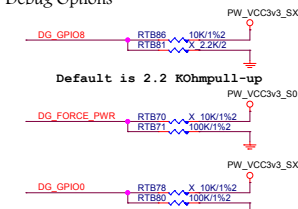
OR:0
0.1uF:0
1uF:1
4.7uF:0
10uF:0
22uF:0



HW Pull-Up/Pull-Down



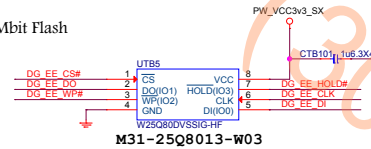
Debug Options



TR JTAG(Remove header)



8Mbit Flash



Place as close as possible to pins

+/- 0.5%

CTB13 18p50N4

CTB14 18p50N4

AN_XTAL_25M_XI

AN_XTAL_25M_XO

YTB1 25MHz220p_S-HF-1

AVL:D04-1003400-F07 要移除

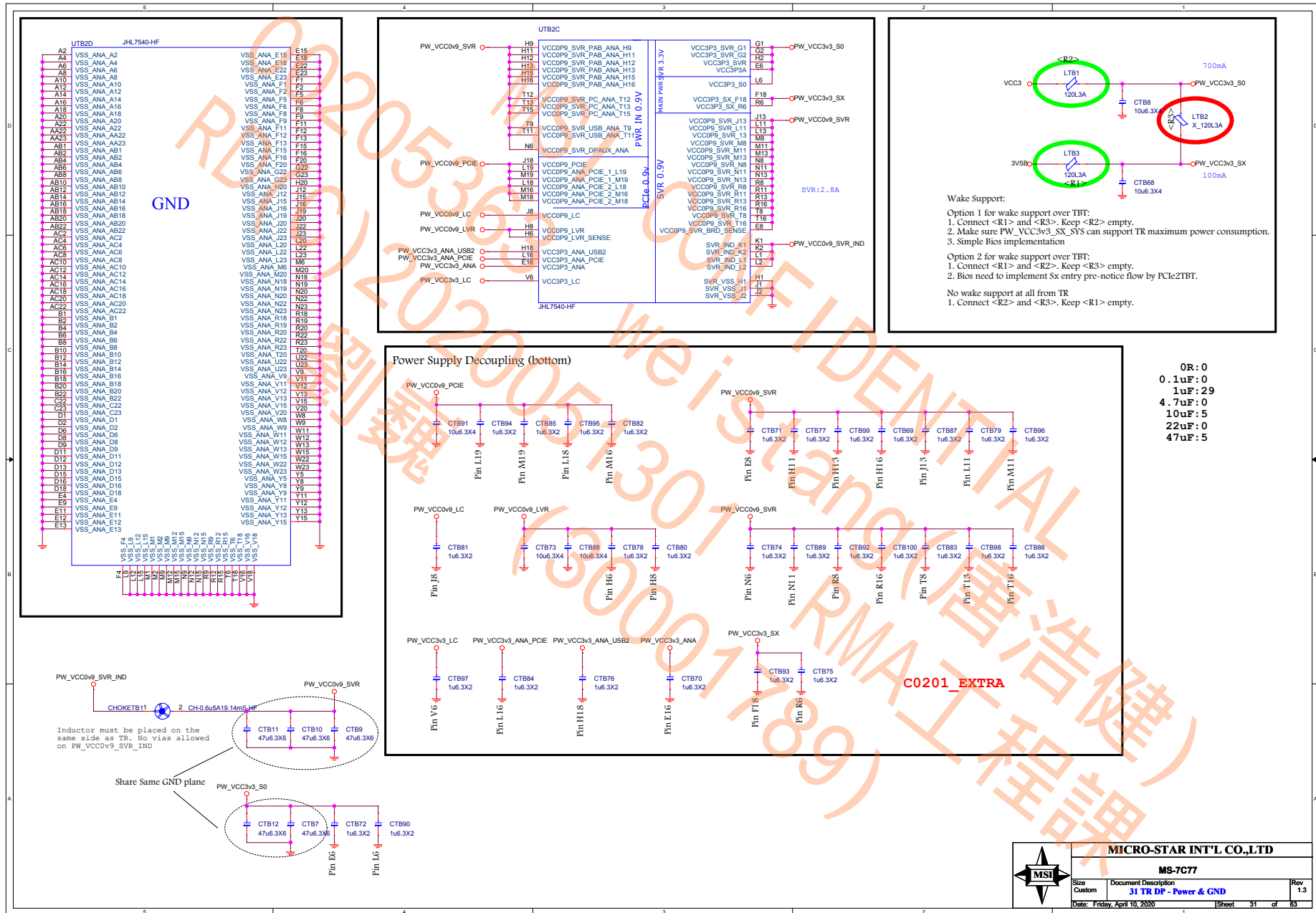


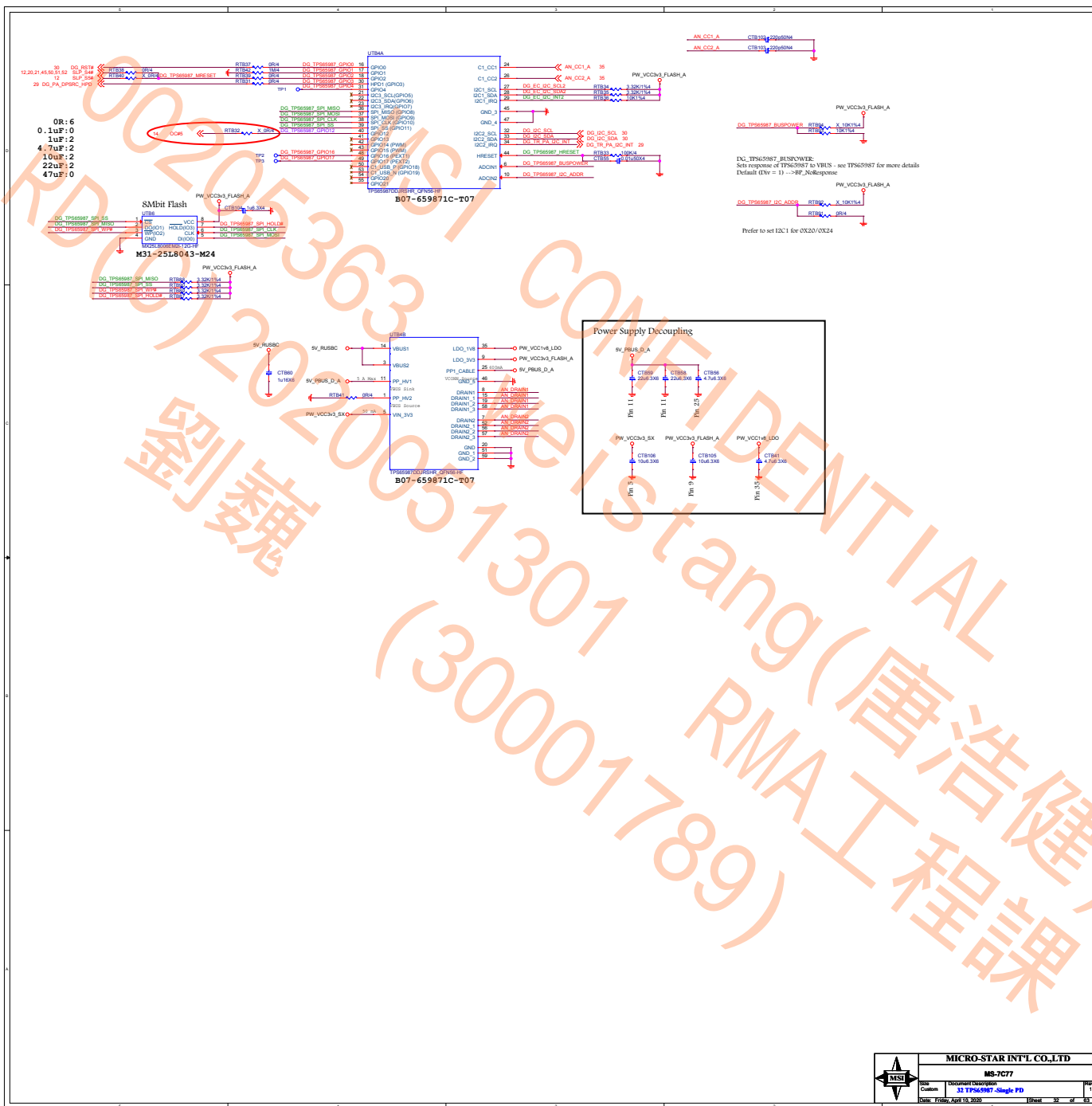
MICRO-STAR INT'L CO.,LTD

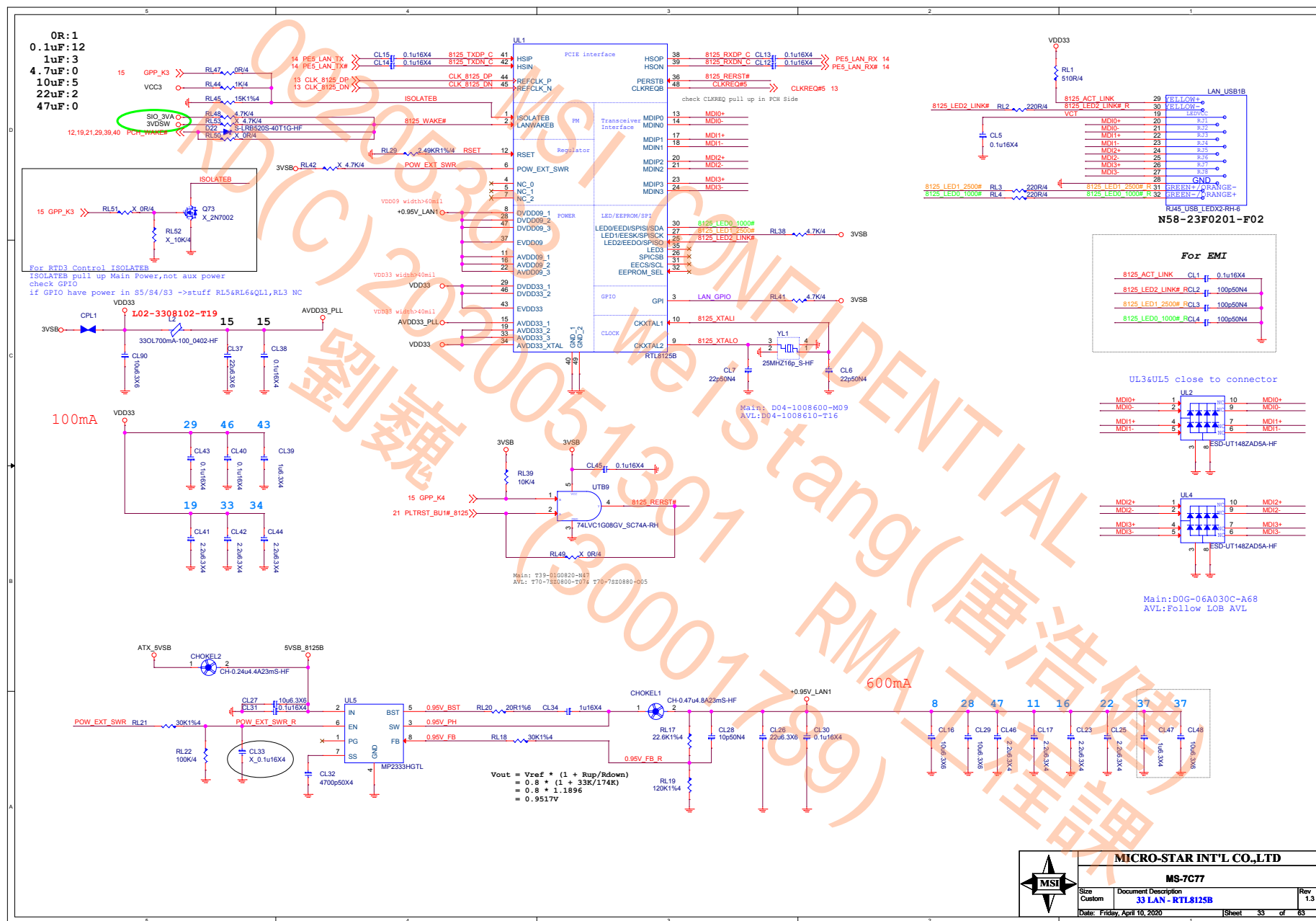
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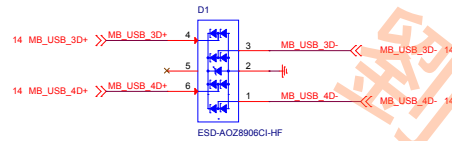
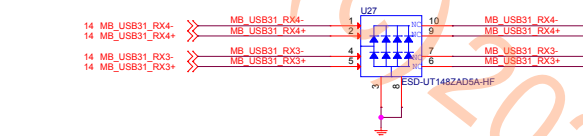
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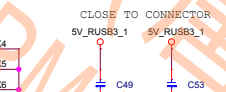
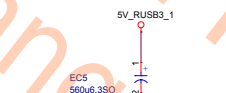
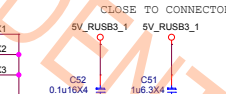
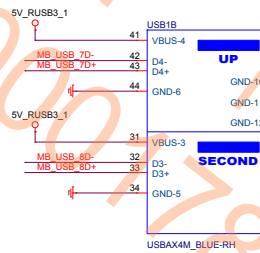
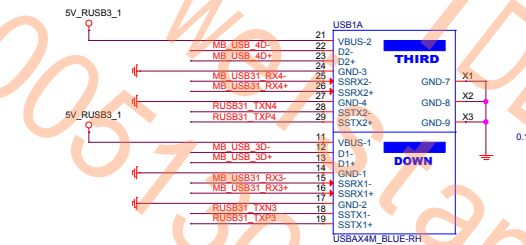
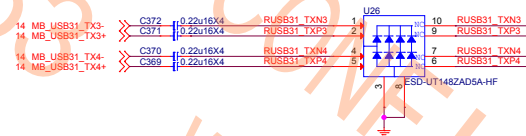
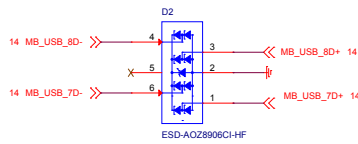




OR: 0
0.1uF: 2
1uF: 2
4.7uF: 0
10uF: 0
22uF: 0
47uF: 0



ESD Protection
NEAR CONNECTOR
D0G-05A0529-A68



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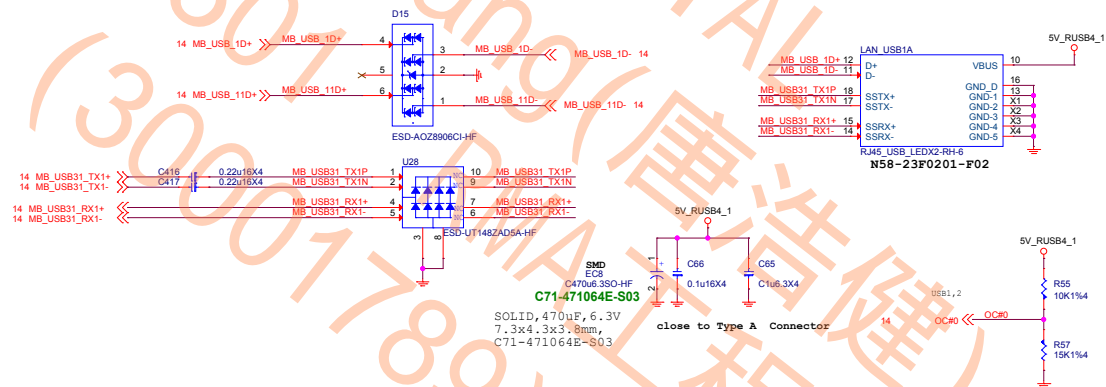
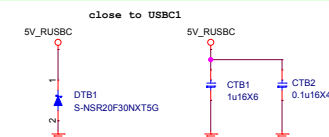
MS-7C77

Size Custom Document Description 34 Rear LAN USB3.1&USB2.0 Rev 1.3
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The diagram shows a detailed PCB layout with various components and their connections:

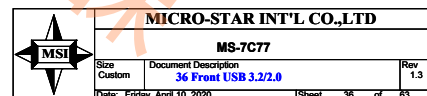
- Resistors:** DTB4 A, DTB3 A, DTB5 A, DTB2 A, DTB1 S-NSR20F30NXT5G, CTB1 1u16X.
- Capacitors:** C416 0.22u16X4, C417 0.22u16X4, ESD-U1148ZAD5A-HF, C470u6.350-HF, C66 0.1u16X4, C65 C1u6.3X4.
- Connectors:** USB31_TX1P, MB_USB31_TX1P, MB_USB31_TX1N, MB_USB31_RX1+, MB_USB31_RX1-, MB_USB31_TX1N, MB_USB31_RX1+.
- Other Components:** AN_CC1_A, AN_CC2_A, DG_PA_SBU1, DG_PA_SBU2, AN_CC1_A, AN_CC2_A, DG_PA_SBU1, DG_PA_SBU2, AN_CC1_A, AN_CC2_A, DG_PA_SBU1, DG_PA_SBU2.

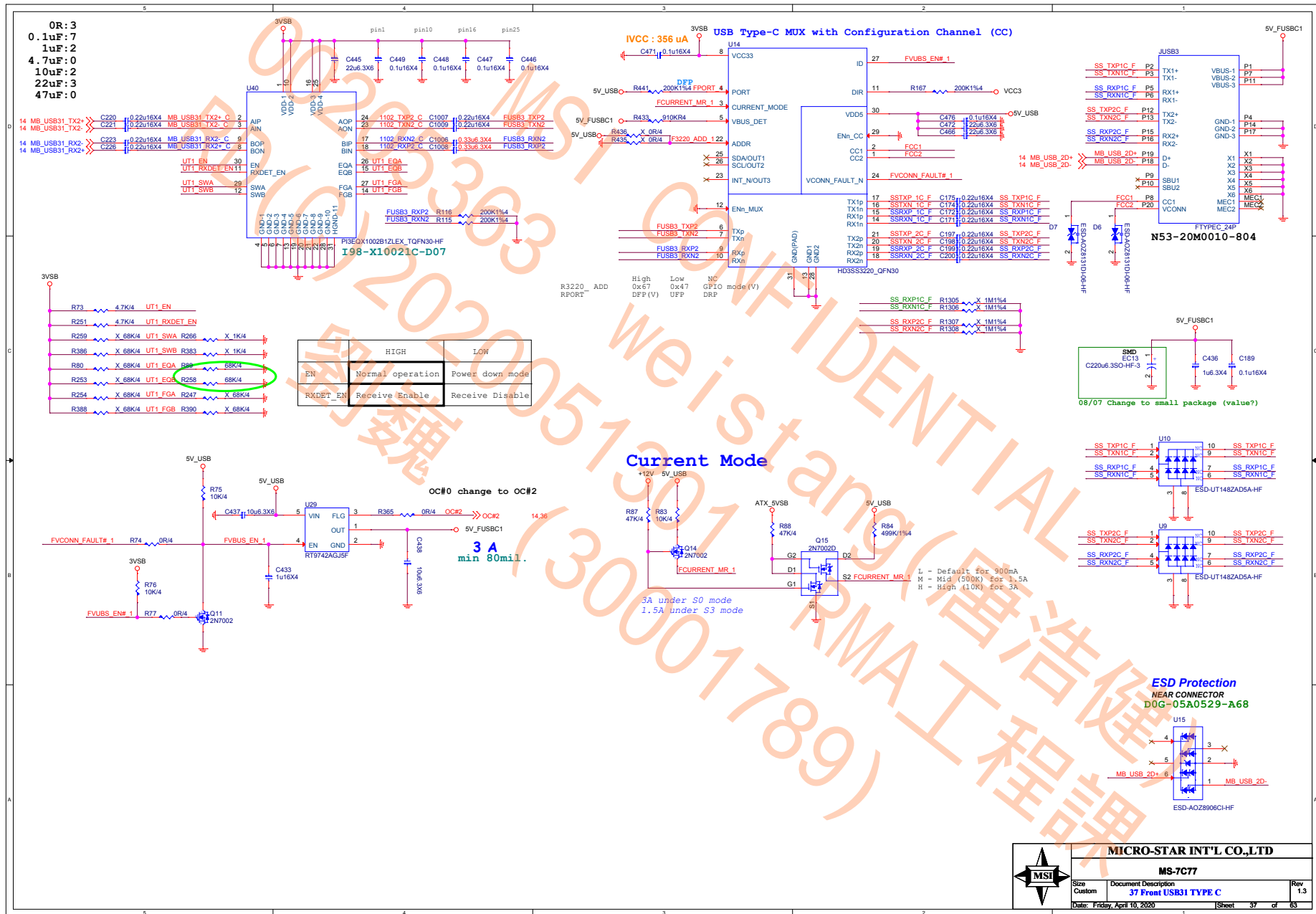
The diagram also includes a legend for the components and their values, such as "check footprint" and "close to Type A Connector".



Size Custom	Document Description 35 Rear-USB31 TYPEA+TYPE C
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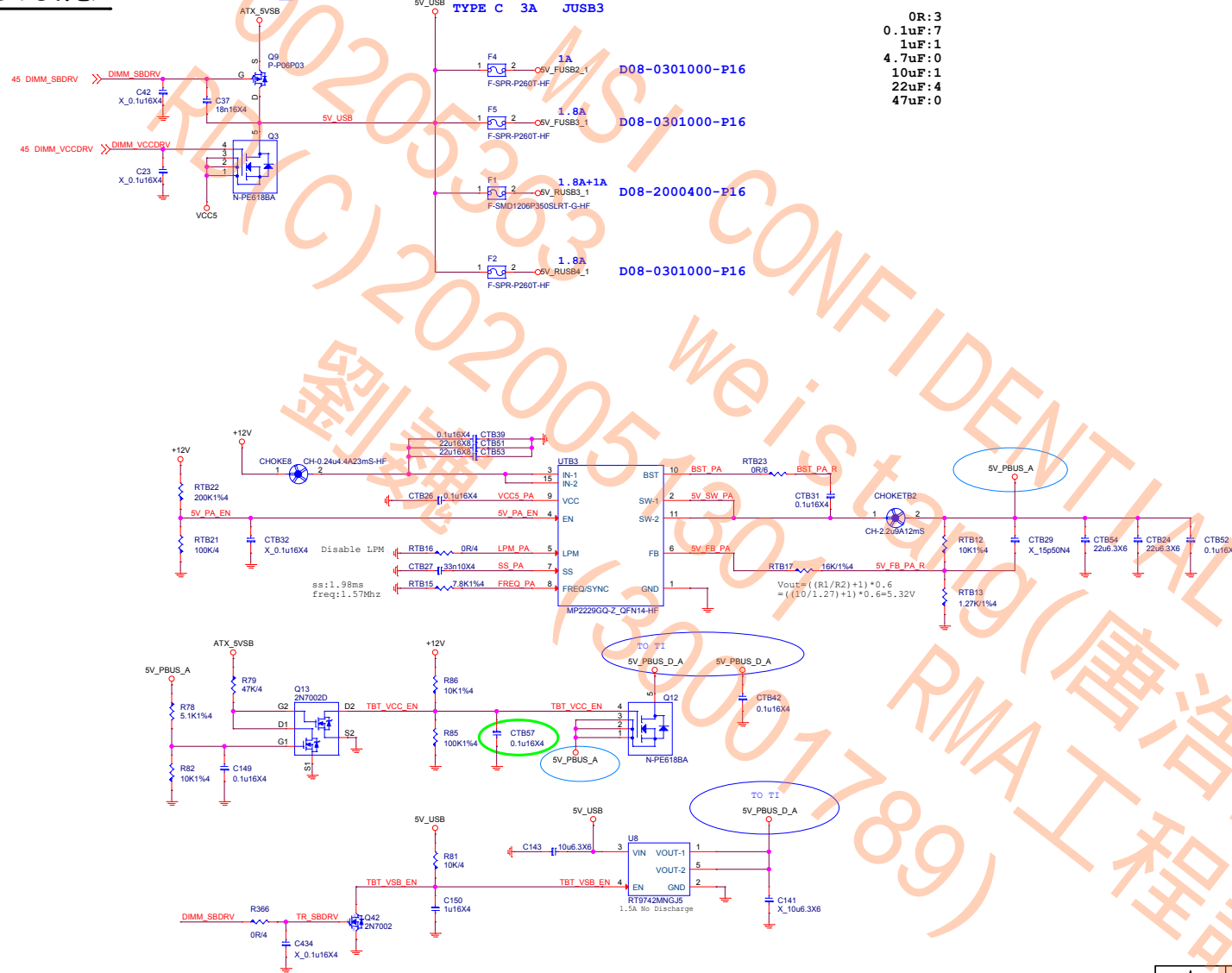
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USB POWER

5V_USB:10.4A



0R:3
0.1uF:7
1uF:1
4.7uF:0
10uF:1
22uF:4
47uF:0

D08-0301000-P16

D08-0301000-P16

D08-2000400-P16

D08-0301000-P16

D08-0301000-P16

D08-0301000-P16

D08-0301000-P16

D08-0301000-P16

D08-0301000-P16

D08-0301000-P16

D08-0301000-P16

D08-0301000-P16

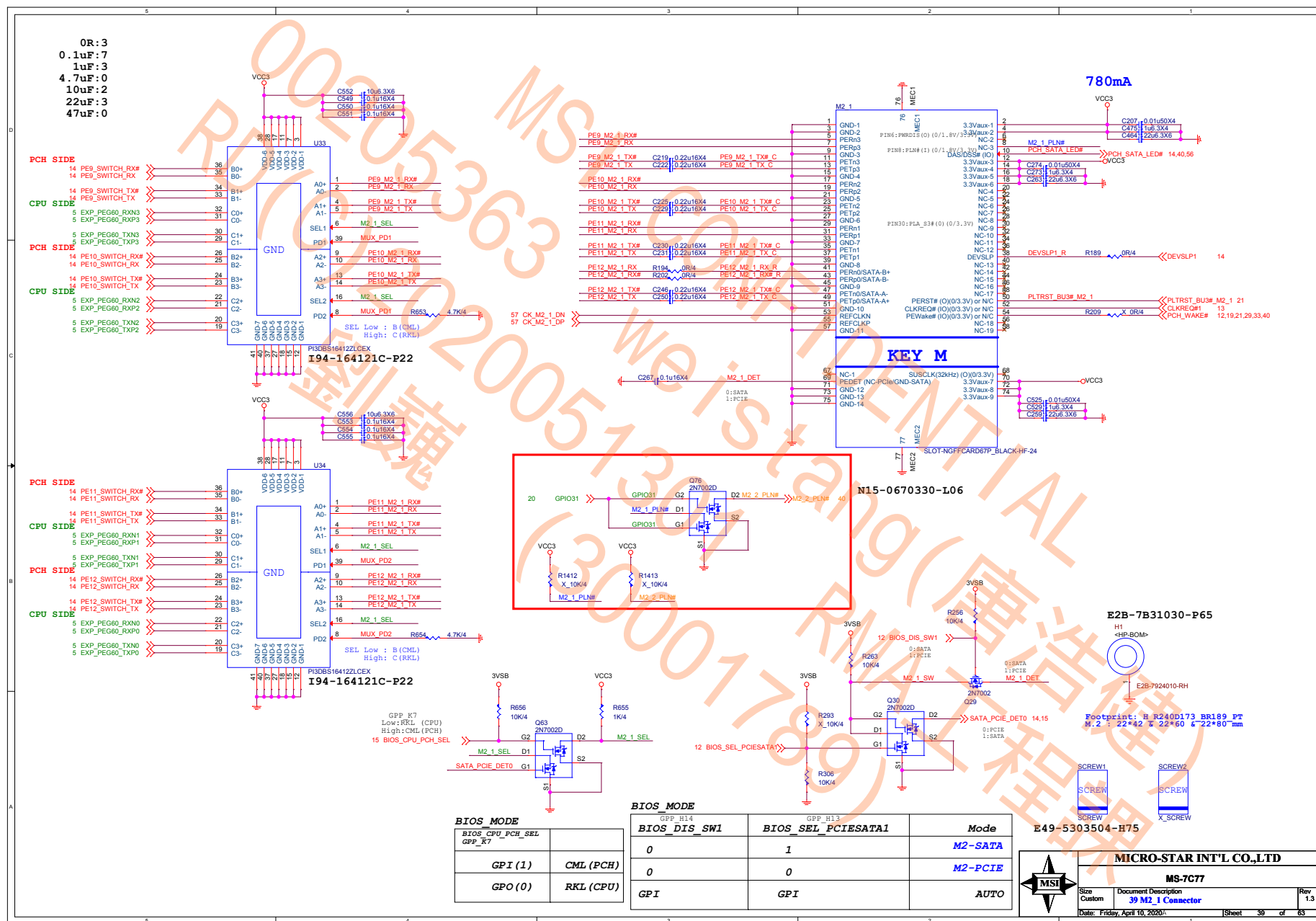
D08-0301000-P16

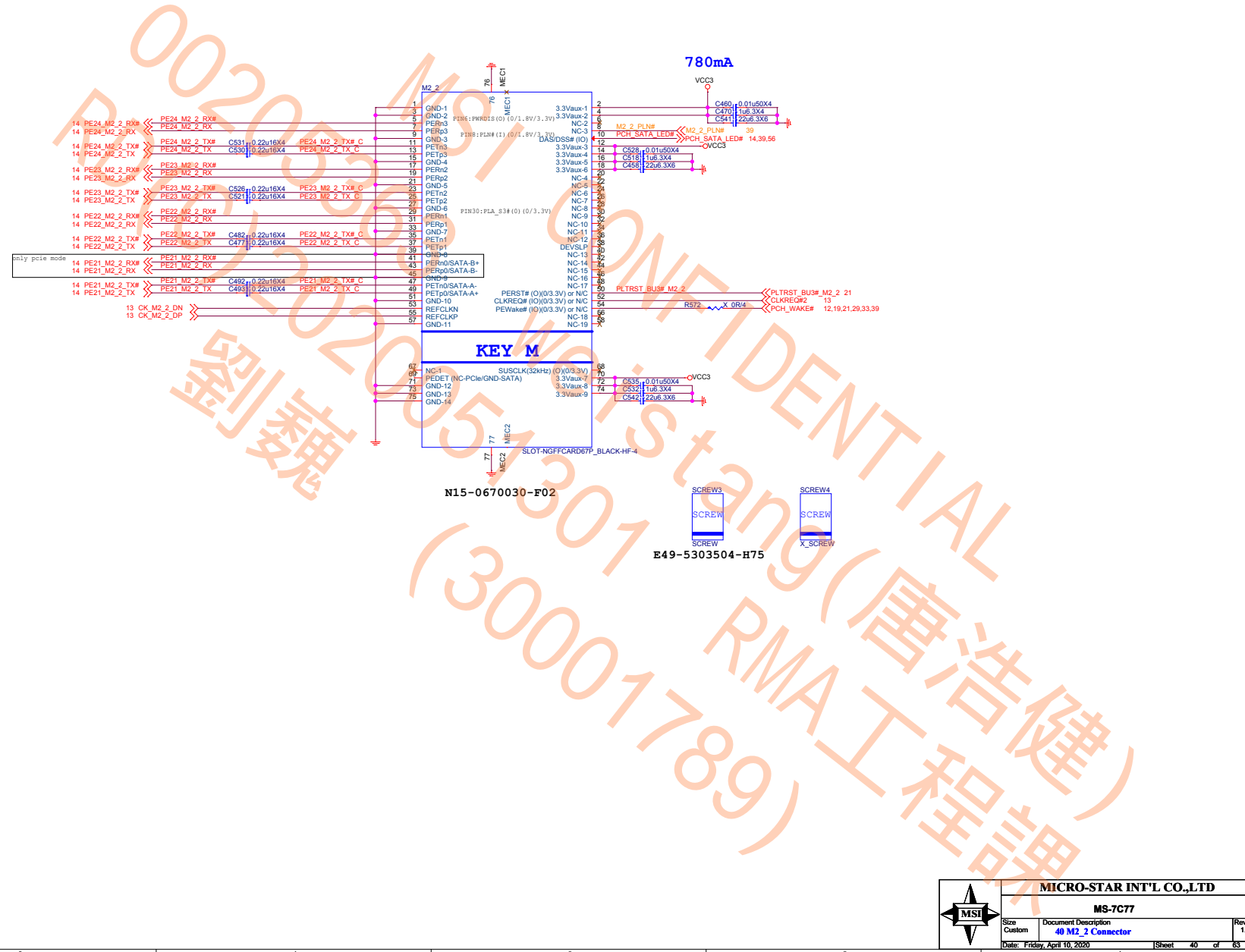
D08-0301000-P16

D08-0301000-P16

D08-0301000-P16

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[illegible]

E49-5303504-H75

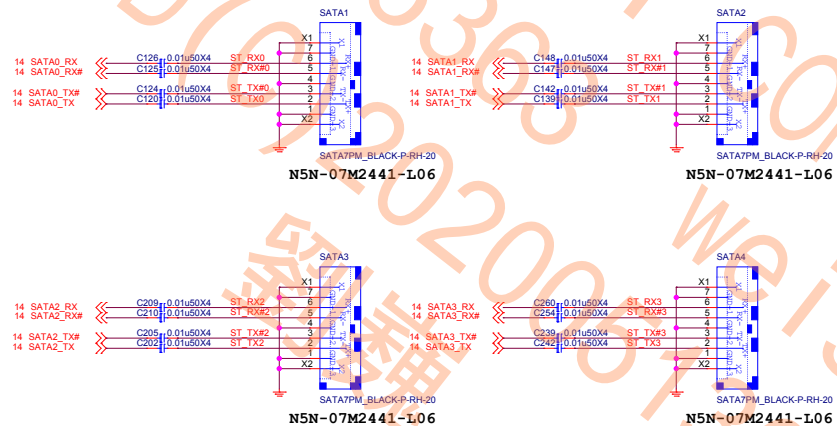


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SATA GEN3



support BT&WIFI, not support LTE

0R:15
0.1uF:2
1uF:0
4.7uF:0
10uF:2
22uF:0
47uF:0

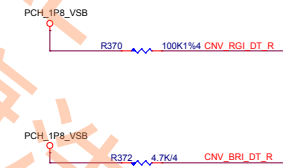
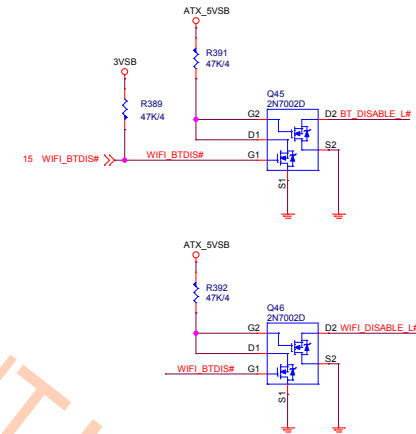
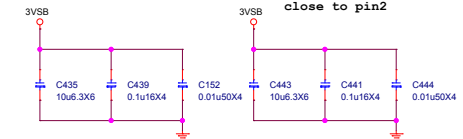
KEY E

COVER1
VR
Cover
X1
X2
X_E21-4442021-RH
TOP E21-7C73020-C22
BOT E21-7C73010-C22
Footprint WIFI_MODULE_37_7X35_4

Wireless1
INTEL-8265
Wireless
604-4467-030

SLOT:NGFFCARD67P_BLACK-HF-46
N15-0670610-L06

1.36A PEAK CURRENT 9560



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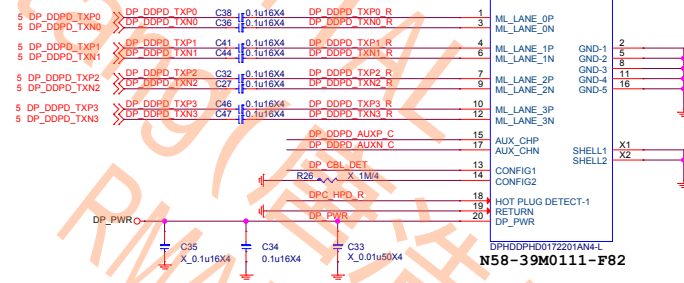
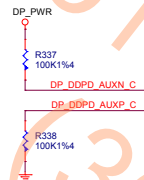
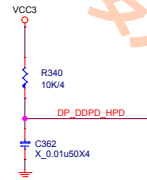
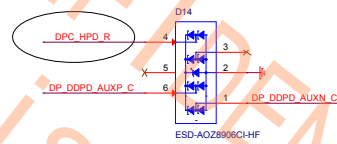
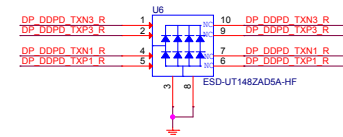
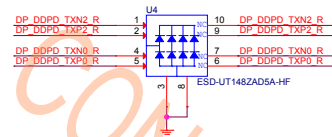
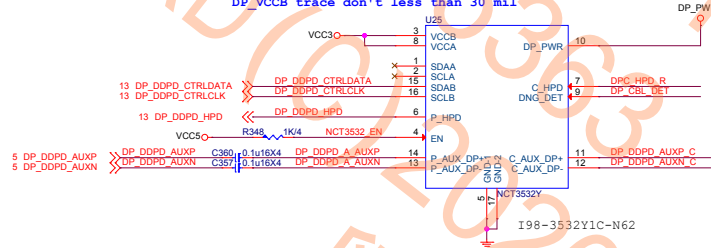
```

0R:0
0.1uF:11
1uF:0
4.7uF:0
10uF:1
22uF:0
47uF:0

```

500mA

DP_VCCB trace don't less than 30 mil



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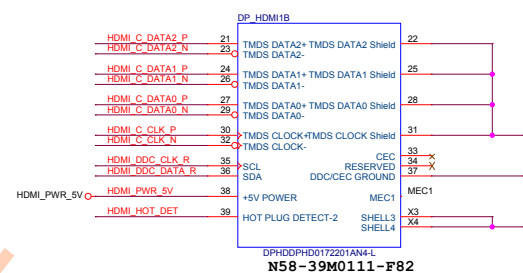
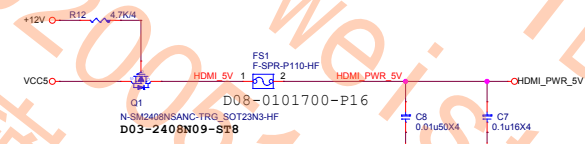
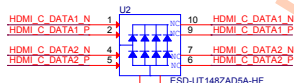
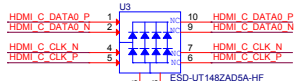
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5	HDMI_D0BP_CLK_P	C17	0.tu16x4	HDMI_C_CLK_P	R19	470R4	HDMI MOS DAT
5	HDMI_D0BP_CLK_N	C18	0.tu16x4	HDMI_C_CLK_N	R21	470R4	
5	HDMI_D0BP_TX2_P	C1	0.tu16x4	HDMI_C_DATA2_P	R1	470R4	
5	HDMI_D0BP_TX2_N	C16	0.tu16x4	HDMI_C_DATA2_N	R4	470R4	
5	HDMI_D0BP_TX1_P	C6	0.tu16x4	HDMI_C_DATA1_P	R7	470R4	
5	HDMI_D0BP_TX1_N	C9	0.tu16x4	HDMI_C_DATA1_N	R14	470R4	
5	HDMI_D0BP_TX0_P	C26	0.tu16x4	HDMI_C_DATA0_P	R27	470R4	
5	HDMI_D0BP_TX0_N	C25	0.tu16x4	HDMI_C_DATA0_N	R24	470R4	

[illegible]

The schematic diagram shows the HDMI C block with the following connections:

- HDMI C CLK_N** is connected to **R22** (X_180R1%).
- HDMI C CLK_P** is connected to **R22** (X_180R1%).
- HDMI C DATA0_N** is connected to **R25** (X_180R1%).
- HDMI C DATA0_P** is connected to **R25** (X_180R1%).
- HDMI C DATA1_N** is connected to **R11** (X_180R1%).
- HDMI C DATA1_P** is connected to **R11** (X_180R1%).
- HDMI C DATA2_N** is connected to **R2** (X_180R1%).
- HDMI C DATA2_P** is connected to **R2** (X_180R1%).



7501 Mode
:Support S0/S3/S5
L:Support S0/S3

0R: 4
0.1uF: 7
1uF: 3
4.7uF: 0
10uF: 2
22uF: 3
47uF: 0

For S5-G3 can ramp issue

The top diagram illustrates the 3V3SW power supply circuit. It starts with an ATX_5VSB input, which passes through a voltage divider consisting of resistor R417 (47K/4) and capacitor C474 (10u6 3X6) to the VIN pin of the DC-DC converter U31 (GS7133SSO-R_PSOP8-HF, AVL:I31-3730S02-N62). The converter's VOUT pin is connected to the 3V3SW output. The feedback (FB) pin is connected to a network of capacitors (C456, 10p500N4) and resistors (R410, 31.6KR1%4; R408, 10K1%4). The output is further filtered by capacitors C463 (10u6 3X6) and C465 (0.1u16X4).

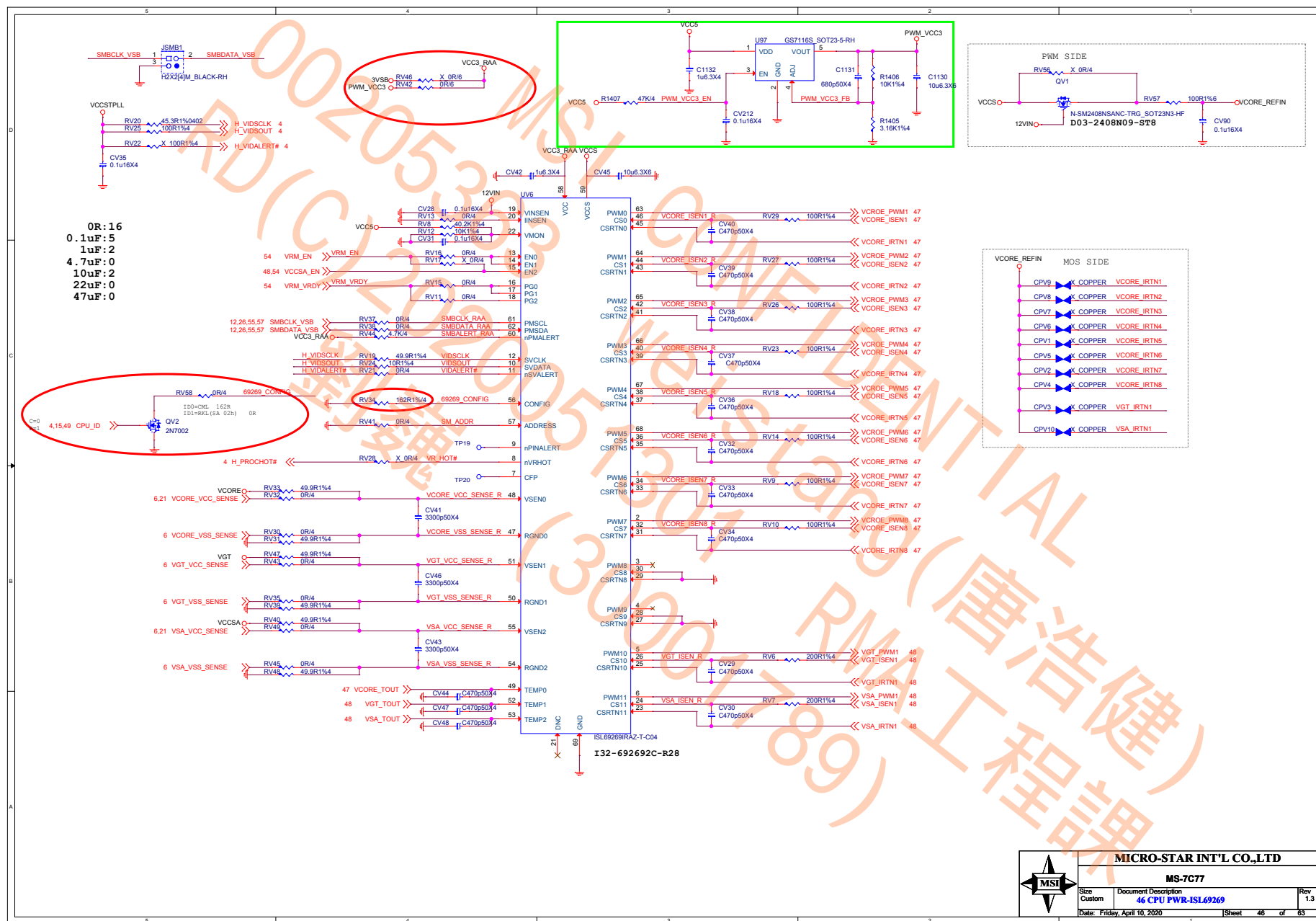
The bottom diagram shows an alternative or simplified circuit for the 3V3SW supply. It uses a voltage divider (R387, 47K/4) connected to ATX_5VSB. The divider's output is connected to the gate of a MOSFET Q48 (2N7002D) through resistor R392 (47K/4). The MOSFET's source is connected to ground, and its drain is connected to the 3V3SW output. The MOSFET is controlled by VSB_ENABLE# and SIO_3VA signals through a network of resistors (R392, Q47, 2N3904) and a capacitor (C457, X_0 1u16X4).

The schematic shows the internal components and connections of the TPS566235. Key features include:

- Input Section:** VIN connected to SW, with a 3VSB_EN signal at pin 5. A 3VSB_PHASE signal is also present.
- Control Section:** PGND-1, PGND-2, PGND-3, and AGND pins are shown. The MODE pin is configured for Sourcing Current mode.
- Output Section:** BST pin connected to FB, which is tied to a feedback network consisting of R248 (1R5%) and C264 (2700pF) snubber. The output is filtered by R229 (91K), R231 (20K), and C270 (22uF).
- Power Stages:** Includes MOSFETs Q21 (N7020D) and Q25 (2N3904), along with various resistors like R123 (47K), R155 (0R4), R216 (100K), and R236 (0R4).
- Capacitors:** Various electrolytic capacitors (C215, C240, C245, C270, C285, C286, C287) and ceramic capacitors (C264, C187) are used for filtering and timing.



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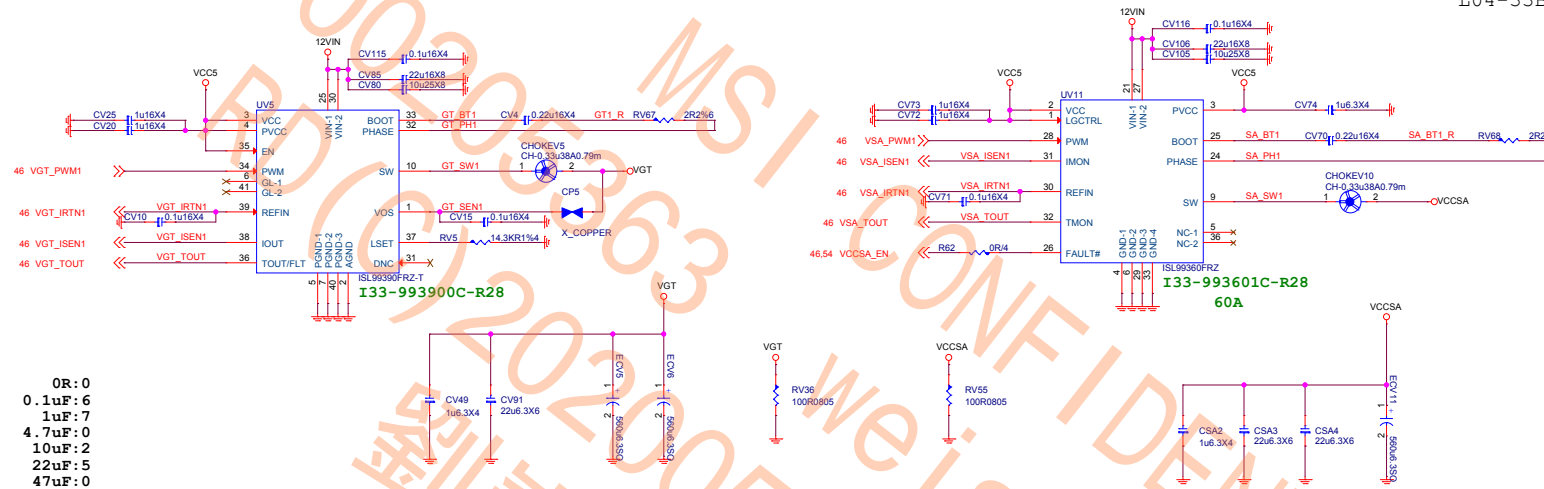
Size Custom	Document Description 46 CPU PWR-ISL69269
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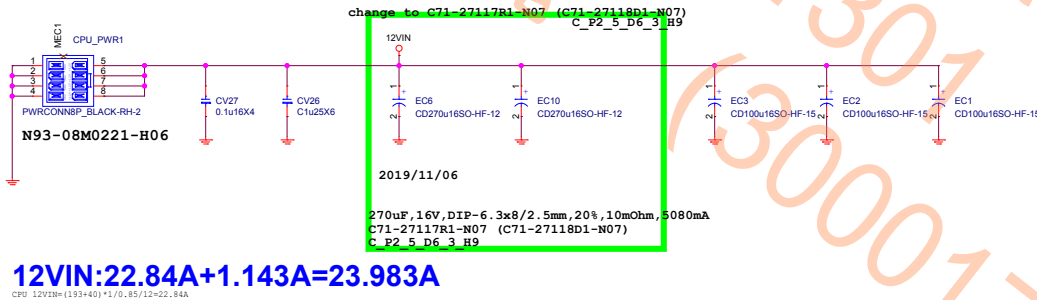
Date: Friday, April 10, 2020



L04-33B7440-T15==0.33



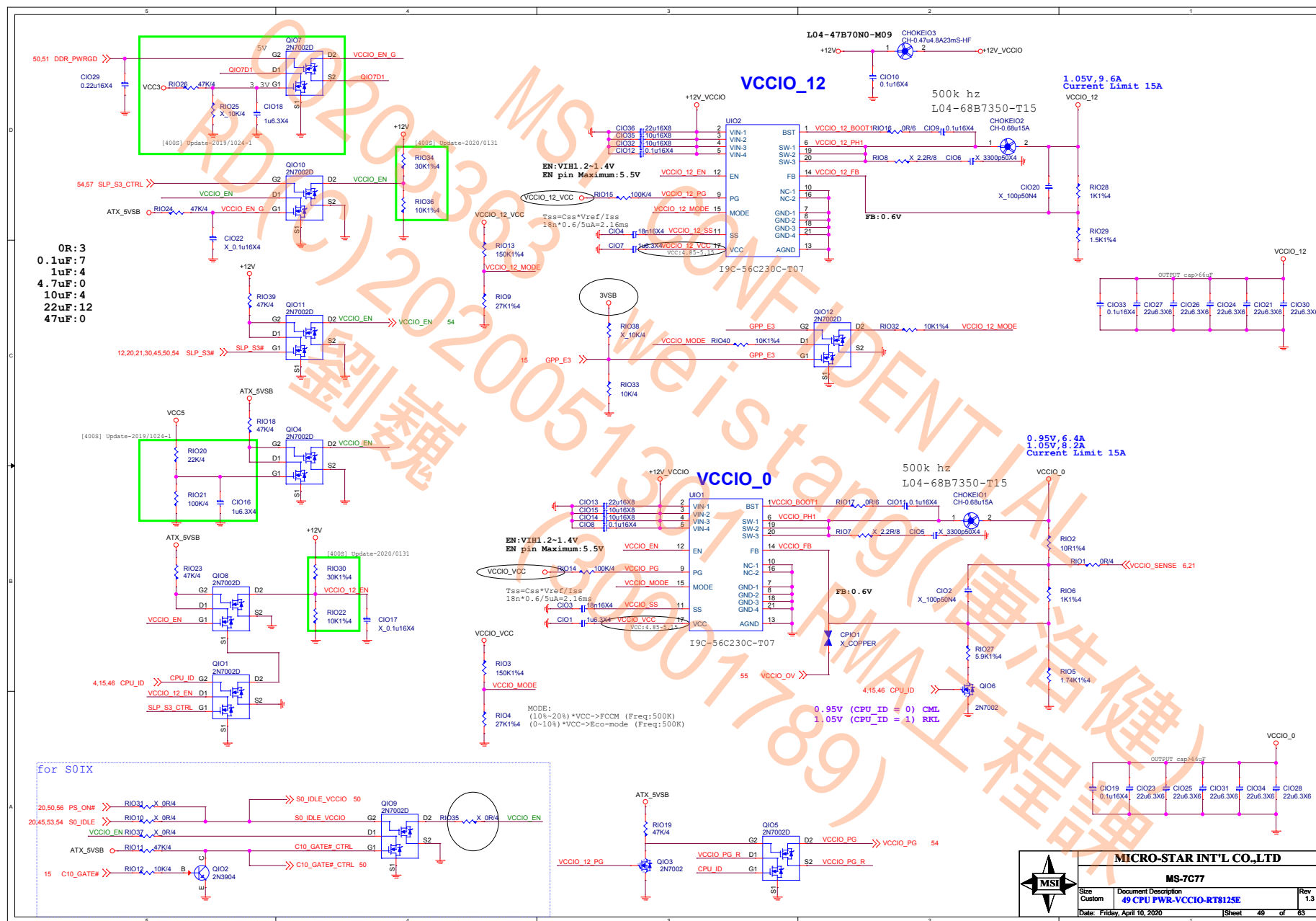
CPU Power connector

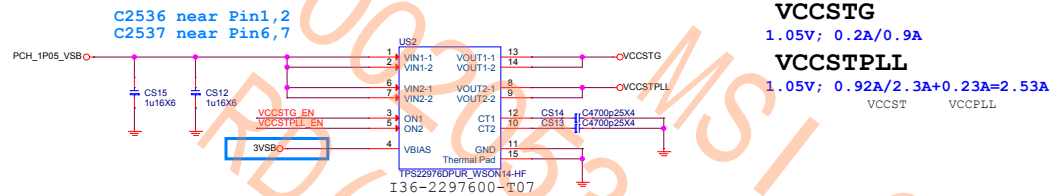


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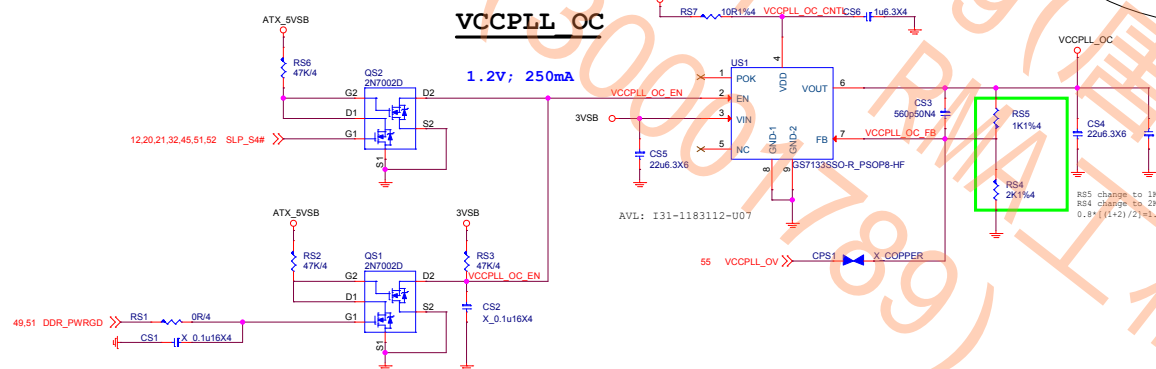
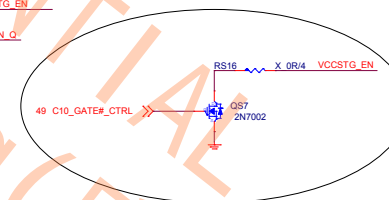
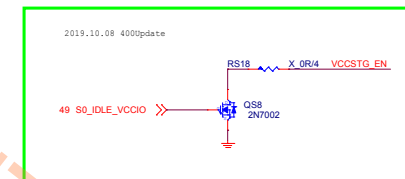
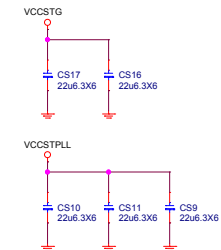
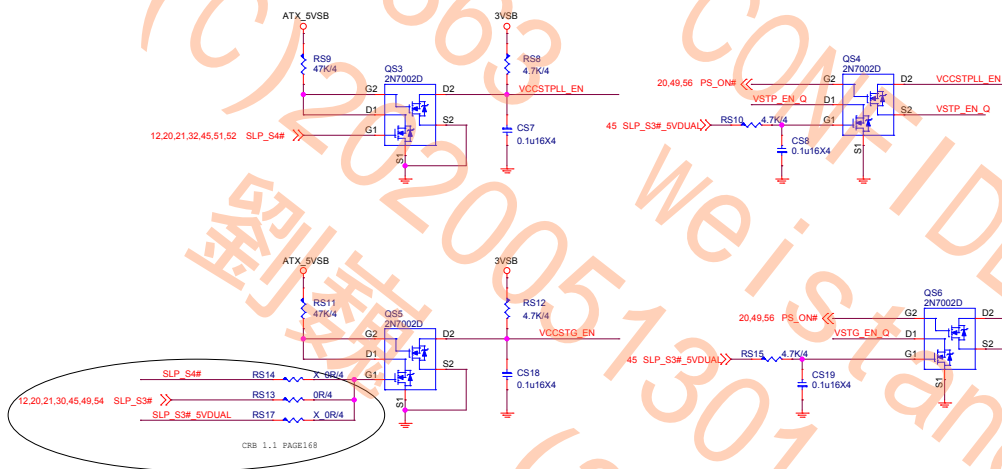
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0R:2
0.1uF:4
1uF:4
4.7uF:0
10uF:0
22uF:7
47uF:0



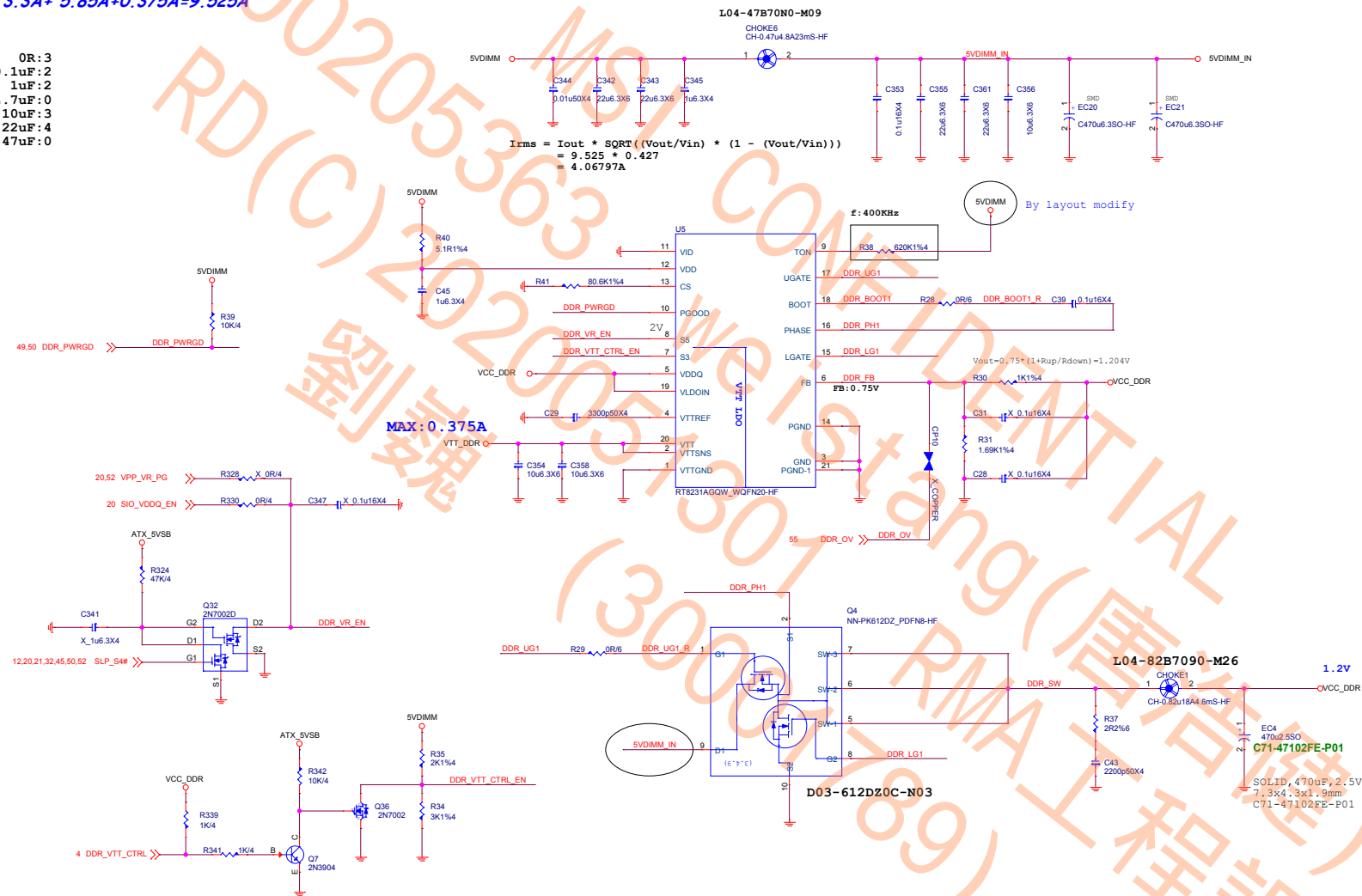
$$3.3A + 5.85A + 0.375A = 9.525A$$

```

0R:3
0.1uF:2
1uF:2
4.7uF:0
10uF:3
22uF:4
47uF:0

```

```
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
      = 9.525 * 0.427
      = 4.06797A
```



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VPP Power:2.5V; 1.12A FOR 2DIMM

OR:2
0.1uF:3
1uF:3
4.7uF:0
10uF:2
22uF:4
47uF:0

VPP25 Power 2.5V; 1.12A

I9C-2333H09-M03

L04-47B70N0-M09

Table 2: Parameters Selection for Common Output Voltages, $V_{IN} = 5V$

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	RT (kΩ)	L (μH)
1.0	33	133	120	1.5
1.2	40.2	82	75	1.5
1.5	40.2	45.3	47	2.2
1.8	40.2	32.4	36	2.2
2.5	40.2	19.1	24	2.2
3.3	40.2	13	30	1.5
5 ⁽¹⁰⁾	40.2	7.68	15	2.2

1.12A

Close to DIMM

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. EN is clamped internally using a 2.8V series Zener diode (see Figure 2). Connecting the EN input through a pull-up resistor to V_{IN} limits the EN input current below 40μA to prevent damage to the Zener diode. For example, when connecting a 604kΩ pull-up resistor to 12V V_{IN} , $I_{Zener} = (12V - 2.8V) / (604kΩ + 35kΩ) = 14μA$.

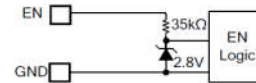


Figure 2: Zener Diode between EN and GND



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D03-612DZ0C-N03 2.2~3.1mohm@5V
OCP=1.6A*1.3=20.8A

```

IOCSET=10uA
OCP_max=Iocset*Rocset/Rdson (min)
        =10uA*6.8k/2.2mohm
        =21.9A

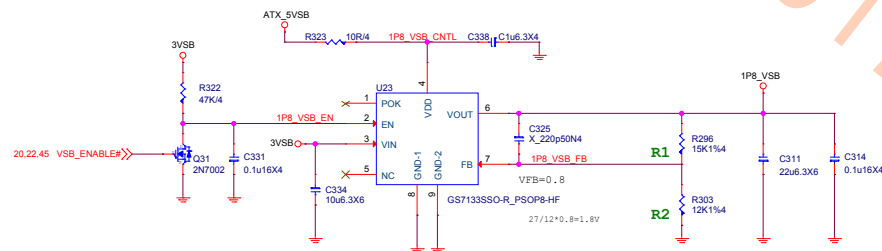
OCP_max=Iocset*Rocset/Rdson (min)
        =10uA*6.8k/2.2mohm
        =21.9A

```

```

0R:4
0.1uF:4
1uF:2
4.7uF:0
10uF:4
22uF:3
47uF:0

```

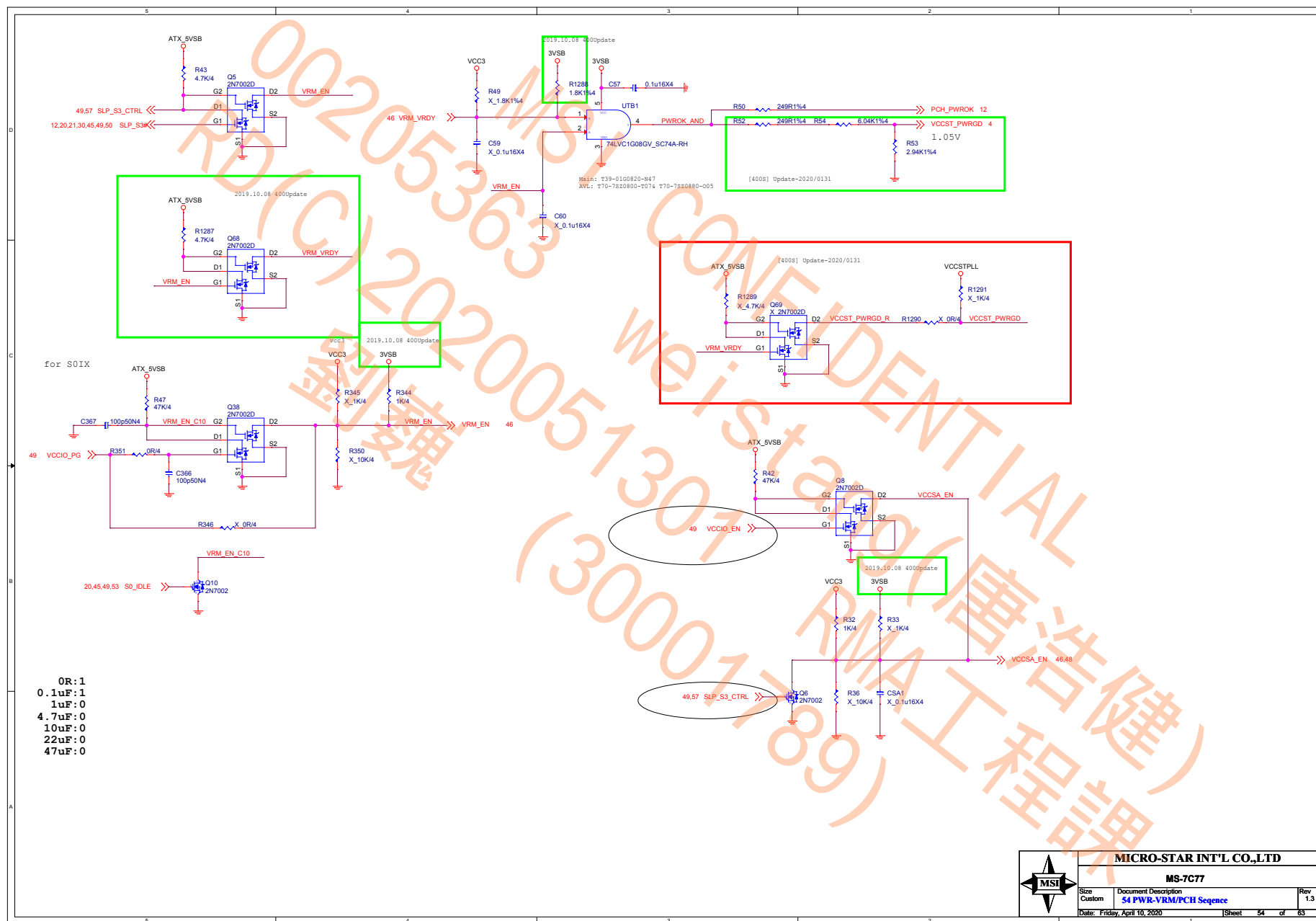


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Size	Document Description
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Custom	53 PCH POWER-RT8125E/1P8_VSB	1.3
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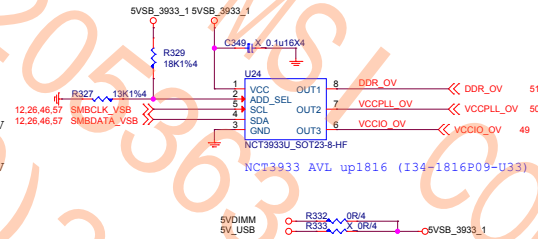


0R:1
0.1uF:0
1uF:0
4.7uF:0
10uF:0
22uF:0
47uF:0

NCT3933 source 10uA
 $V_{out} = [V_{REF} * (1 + R173/R1056)] + 10uA * R173$
 $= 0.75V * (1 + 1K/3.16K) + 10uA * 1K = 1.204V + 0.010V = 1.214V$
NCT3933 sink 10uA
 $V_{out} = [V_{REF} * (1 + R173/R1056)] - 10uA * R173$
 $= 0.75V * (1 + 1K/3.16K) - 10uA * 1K = 1.204V - 0.010V = 1.194V$

UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



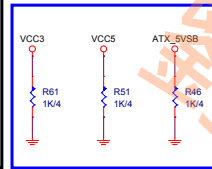
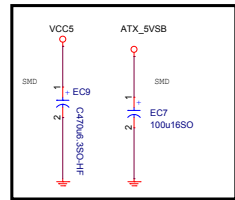
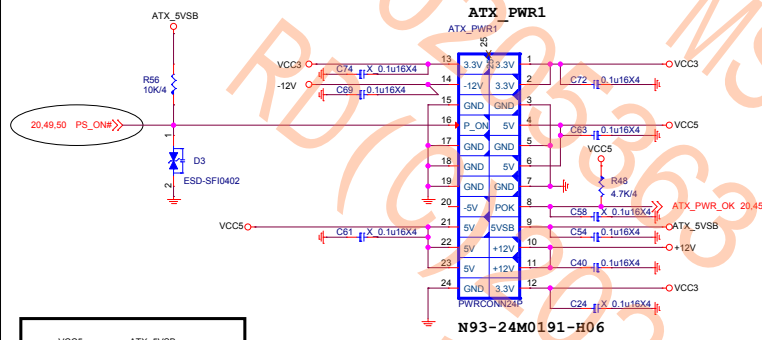
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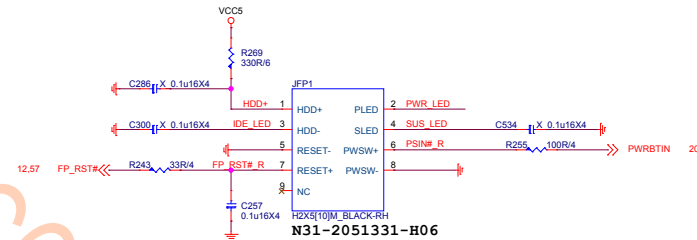
Size	Document Description	Rev
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ATX POWER CONNECTOR

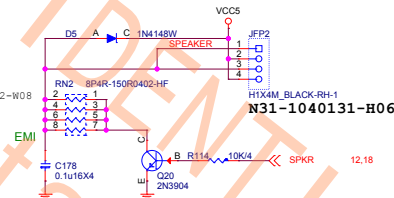
note: If -12V/-5V pin were connected, remember add MLCC cap close pin



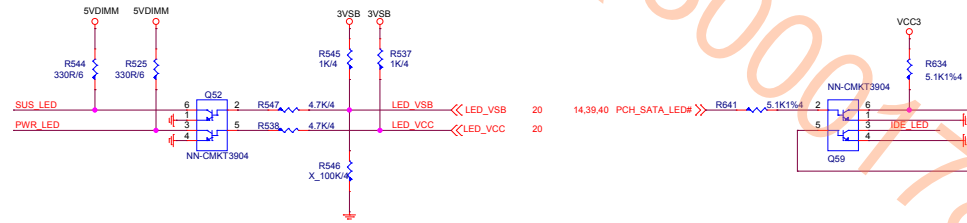
FRONT PANNEL



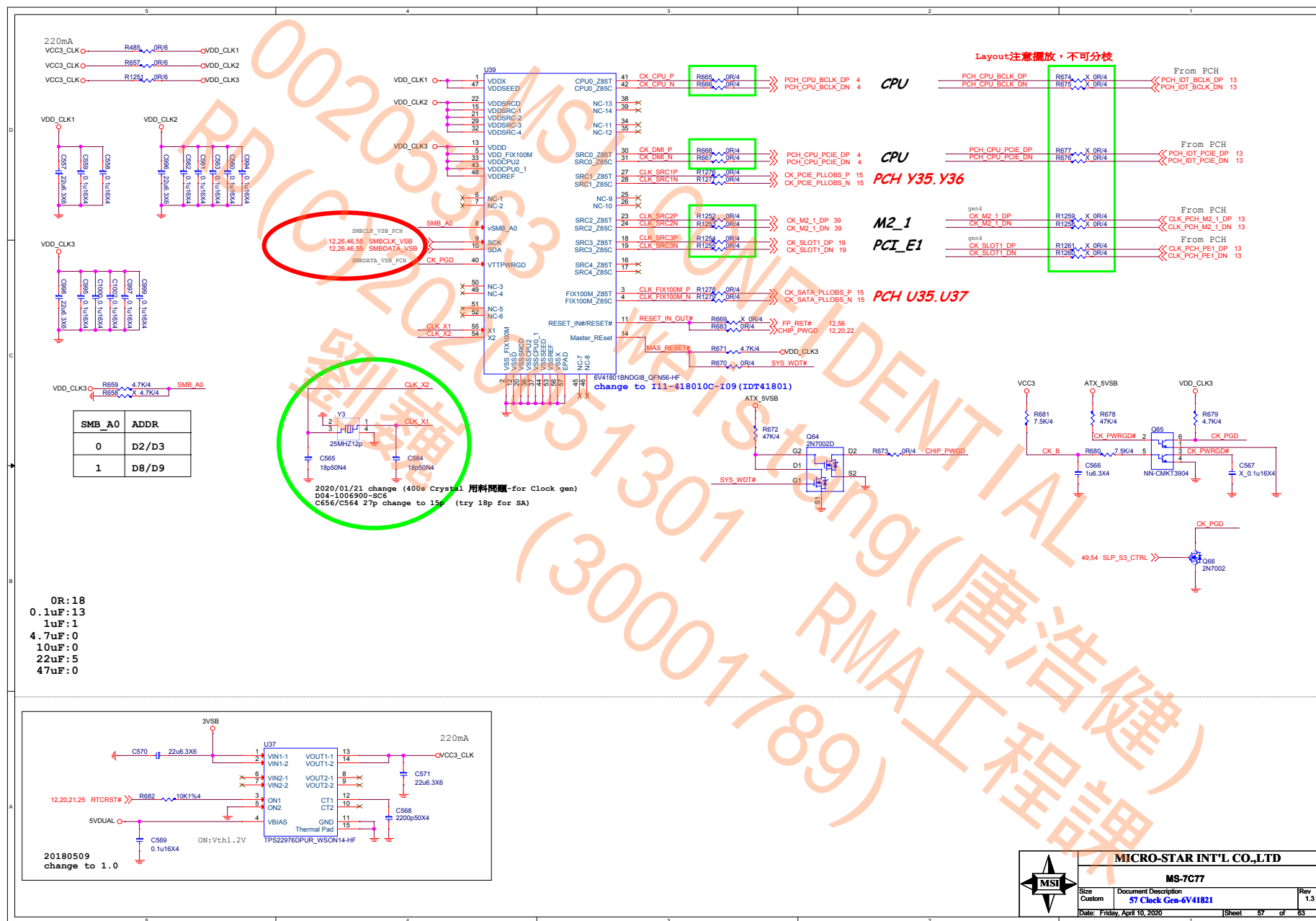
Speaker Pin Header

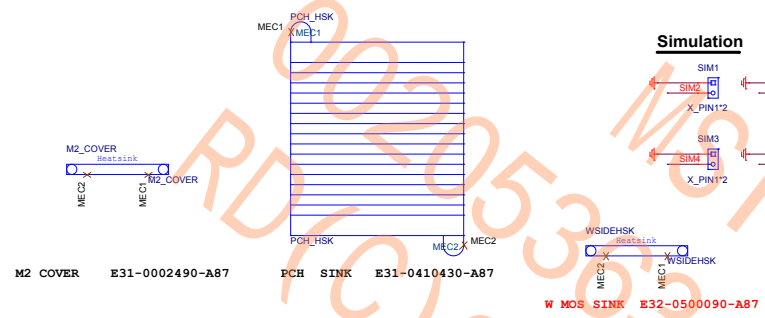


FRONT PANEL LED

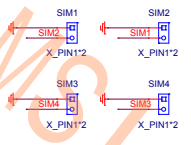


0R:18
0.1uF:7
1uF:0
4.7uF:0
10uF:0
22uF:5
47uF:0

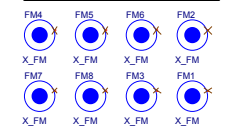




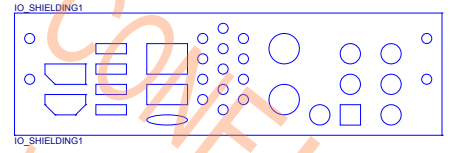
Simulation



Optical Fiducial Marks-120



E22-7C71020-C22



Mounting Holes

